

Service documentation

Receiver type series EKD 500

EKD 511/type 1340.42 A1

EKD 512/type 1340.42 A2

Volume 1

To go with this:

Service documentation 1340.042-91700 Su 02, Vol. 2

We reserve the right to make modifications to the construction and design which serve the improvement and development of our equipment without prior notice.

Order-No. of the Service documentation 1340.042-91700 Su 02
Edition 2/1989
Volume 1

<u>Contents</u>	<u>Page</u>
1. General remarks	5
2. Test equipment and auxiliary testing means	7
3. Hints for dismounting and mounting	9
4. Hints for troubleshooting	11
5. Localization of the faulty subassembly and reestablishment of the functionality of the receiver by subassembly exchange	15
5.1. Check "power supply section"	17
5.2. Check "control unit"	18
5.3. Check "frequency processing"	21
5.4. Check "signal path"	23
6. Repair of the faulty subassembly	26
6.1. Power supply section 1340.039-01500	27
6.1.1. Input and output values	27
6.1.2. Measuring values within the power supply section	28
6.1.3. Troubleshooting table	30
6.2. Control unit 1340.041-01401	34
6.2.1. Function principle	34
6.2.2. Test and check arrangements	37
6.2.3. Repair sequence "local operation"	38
6.2.4. Repair sequence operation "external"	39
6.2.5. Control computer	40
6.2.6. Input-output logic	42
6.2.7. Keyboard	44
6.2.8. Digital display	47
6.2.9. Register and interface	48
6.3. Frequency processing	55
6.3.1. Troubleshooting sequence	55
6.3.2. Frequency processing - outline	56
6.3.3. Phase-lock loop 1 (PLL1)	58
6.3.4. Oscillator 1	60
6.3.5. Frequency divider 1	64
6.3.6. Oscillator 3 (PLL3)	66

<u>Contents</u>	<u>Page</u>
6.3.7. Phase-lock loop 2 (PLL2)	70
6.3.8. Oscillator 2	72
6.3.9. Frequency divider 2	76
6.4. Signal path	78
6.4.1. Check or correction of levelling	78
6.4.1.1. Basic amplification "signal path 1"	78
6.4.1.2. Control volume "signal path 1"	78
6.4.1.3. Mixer - symmetry	78
6.4.1.4. Basic amplification "signal path 1 and 2"	79
6.4.1.5. Levelling "A3E"	79
6.4.1.6. Changing AF line levels (max +6 dBm)	79
6.4.1.7. Balancing "control synchronism/channel A and B, manual control"	79
6.4.1.8. Balancing "automatic control/channel A and B"	80
6.4.1.9. Check "control synchronism/channel A and B, automatic control"	80
6.4.1.10. Adjustment "control start/control element 1" (mixer 1)	80
6.4.1.11. Adjustment "trigger - control amplifier"	80
6.4.1.12. Adjustment "short-time detector"	81
6.4.1.13. Balancing "display E "	81
6.4.2. Signal path 1, 1340.041-01311 or -01312	82
6.4.2.1. Preselector 1, 1340.041-01351	83
Preselector 2, 1340.041-01352	
6.4.2.2. Mixer 1, 1340.041-01353	87
Mixer 2, 1340.041-01354	
6.4.3. Signal path 2, 1340.041-01321 or -01322	88
6.4.3.1. Carrier oscillator 1340.037-01355	90
6.4.3.2. IF2/A, 1340.041-01357 or -01367	95
IF2/B, 1340.041-01356 or -01366	
6.4.3.3. Demodulator and AF section, 1340.039-01358	96
6.5. F1B-demodulator, 1340.041-01258	98
6.5.1. Check "input signal"	98
6.5.2. Check "input band-pass"	98
6.5.3. Check "limiter amplifier"	98

<u>Contents</u>	<u>Page</u>
6.4.5. Check "PLL"	98
6.5.5. Check "changeover switch for low passes 100/600 Bd"	99
6.5.6. Check "amplifier"	99
6.5.7. Check "evaluator circuit"	99
6.5.8. Check "line current for teleprinter"	99
6.5.9. Check "holding and capture range of PLL"	99
7. Measuring the main parameters	101
7.1. Frequency accuracy	101
7.1.1. Measuring and correcting; with standard test conditions	101
7.1.2. Check and correction on service conditions	101
7.2. Sensitivity	103
7.3. Amplification control	106
8. Components selected by the manufacturer	109
List of terms translated	110

1. General remarks

For carrying out repair work on receivers of series EKD 500, the following unit-specific documentation is required:

- Equipment documentation series EKD 500 1340.042-91700 Eu 02 (specification, operation, maintenance) forming part of every unit supply.
- Service documentation series EKD 500 1340.042-91700 Su 02
 - Volume 1: Repair instructions
 - Volume 2: Outline of subassemblies
 - Functional diagram
 - Circuit diagrams
 - Complementation drawings

Attention!

When performing service work adhere to the safety instructions especially to those concerning

- * earthing of the unit to be repaired
- * work on open units

Repair work is only to be carried out by authorized and particularly instructed specialists being well acquainted with the analogue and digital integrated circuit engineering as well as with the work of electronic units.

Any person meeting these demands will be able to repair every subassembly.

Reestablishment of troublefree functioning of the receiver can be performed through

- * detecting and replacing the faulty subassembly (Section 5)
- * repairing the faulty subassembly (Section 6)

In case of fault indication (F1 to F4) during ROM test (A5), the complete printed circuit "Control computer" (contained in spare part list E9) is to be replaced.

The spare part assortment offered by the manufacturer is to be taken from the spare part lists which are supplied on special request.

Spare part list E1: mechanical and electrical wear parts.

Spare part list E7: complete spare subassemblies (cassettes, control unit, power supply section)

Spare part list E9: stock spares for unit-specific spare parts

Capacitors, resistors, diodes, transistors, and integrated circuits required for repair work can also be procured from other manufacturers. It is to be observed that the electrical and mechanical values are equivalent. Component replacement on the double-clad pc boards requires utmost care when soldering on the plated-through holes.

If the requirements for subassembly repair are not met, it is recommended to exchange the entire subassemblies and have them repaired in a service workshop.

Performing repair work on the basis of this service documentation requires the test equipment and auxiliary testing means listed below. In the following, the abridged designation of the instruments is used; e.g. RF generator: P4.

- P1 Counting frequency meter
 $f_e \approx 120 \text{ MHz}$
 $\Delta f/f \approx 1 \cdot 10^{-7}$
 $U_e \approx 50 \text{ mV}$
- P2 RF-mV meter with RF measuring head and 50 ohm load
 $f = 10 \text{ kHz to } 200 \text{ MHz}$
 $U_e = 3 \text{ mV to } 10 \text{ V}$
- P3 AF-mV meter
(2x) $f = 5 \text{ Hz to } 200 \text{ kHz}$
 $U_e = 15 \text{ mV to } 5 \text{ V}$
 $R_e \approx 100 \text{ kohm/V}$
- P4 RF generator
 $f = 10 \text{ kHz to } 30 \text{ MHz}$
 $R_i = 75 \text{ ohm}$
 $\text{emf} = 1 \mu\text{V to } 3 \text{ V}$
unmodulated/modulated
 $1000 \text{ Hz } m = 0.3$
- P5 Double-beam oscilloscope
 $f_e \approx 50 \text{ MHz}$
- P6 Single-beam oscilloscope
 $f_B \approx 10 \text{ MHz}$
- P7 Wobble oscillator with display unit and probe
 $f = 100 \text{ kHz to } 200 \text{ MHz}$
- P8 Multimeter
 $R_i \approx 100 \text{ kohm/V}$
- P9 Digital voltmeter
 $U_e \approx 30 \text{ V dc}$

- P 10 Tone oscillator
 - f = 300 Hz to 6000 Hz
 - R_i = 20 ohm
 - U_a = 2 mV to 1 V
 - P 11 Mains control transformer 0 to 250 V/6 A
 - P 12 Line tester
 - P 13 Test plug 'substitution - control unit'
1340.042-01602
 - P 14 Adapter cable 'input-output logic'
1340.042-01603
 - P 15 Connection adapter 'control unit'
1340.042-01604
-
- RF cable (BNC-50 ohm) 2 pcs. 1340.037-01124
 - RF adapter 33 TGL 200-380
-
- 'Test cable set
1340.042-01601
(cf. equipment
documentation
1340.042-01700 Eu 02
Section I 6)
 - } contained in the
accessories
1340.037-10001
Z1 02 (4)

3. Dismounting and mounting

Pull the mains plug before starting dismounting. Loosen the red-ring marked screws provided below the handle of the plug-in. Withdraw the plug-in out of the rack by pressing the laterally arranged latches inwards.

Attention! Place the plug-in directly next to the casing and separate the BNC plug of the aerial cable from the plug-in.

After pulling the mains plug, the electric connection between the plug-in and the casing can be reestablished by means of the 30-core or 8-core adapter cable contained in the accessories.

Upon loosening the 8 screws marked with a red ring located on the right plug-in wall, the power supply section can be withdrawn upwards and connected again with the plug-in via the 16-core adapter cable contained in the accessories. An extractor, forming part of the accessories, (drwg.-No. 1340.037-02823) can be used for this purpose.

For cassette exchange, slacken per cassette 2 wing nuts provided on the rear wall of the plug-in and 2 hexagon screws (SW 8) on the front.

The front plate can be swung down by 90° thus providing access to the connections of all control elements as well as to the cassette terminals by only loosening the two screws located next to the plug-in handles.

For exchanging the "control unit" (with the front plate swung down by 90°), slacken both controls " " (13) and "changeover switch for LED row" (2) as well as the 4 fastening screws. After removing the two plug-and-socket connections X1022 and X1023 the subassembly can be lifted out.

The defective control elements

- * regulator "volume" (4)
- * regulator "RF/AF amplification" (6)
- * regulator "A1/pitch" (5)
- * changeover switch/monitoring channel (3)
- * unit switch ON/OFF (1)

can only be replaced with the "control unit" taken out of the receiver.

Access to all components of the cassettes is provided after loosening the 4 wing screws, swivelling out the two outer cassettes and unscrewing the 4 inner lids (with the pressed-in fastening points).

When a pc board is to be exchanged, take the respective cassette out of the casing and unscrew both lids. On the soldering side, slacken the 4 hexagon nuts by means of a socket wrench (7 mm). On the complementation side, remove the probably existing connections to the adjacent circuit.

The pc board can be withdrawn to the rear.

For carrying out repair work on the inner side of the rear wall of the casing, loosen the 4 hexagon nuts of the rear wall and the earth connections provided on the right inner side of the casing. Then, the rear wall of the casing can be removed.

Mounting is carried out in the reverse order.

4. Hints on troubleshooting

In case of faulty operation, fault localization is necessary for aimed repair work.

The sequence is the following:

- External fault sources in the incoming and outgoing cables are to be excluded by checking.
 - Exclude wrong operation of the receiver.
 - If a total breakdown is present, check the fuse link in the receiver plug-in (equipment documentation EKD 500, section III.6.1.)
 - Check the functionability of the receiver (equipment documentation EKD 500, Section III.5.).
 - Reestablish the functionability of the receiver by:
 - . detecting and replacing the faulty subassembly (Section 5 of this service documentation)
- Recondition: Spare subassembly according to the
 spare part list 1340.042-00001 E7
- . replacing the faulty component
(fault detection acc. to Section 6 of this service documentation)

- Marking of subassemblies:

All subassemblies are marked - in addition to the drwg.-No. - (referred to the electric components) with two-digit numbers. (viz. subassembly survey 1340.042-00001 U 02 (3))

- Marking of components:

All components are marked with four- (five)- digit numbers. The two first digits correspond with the code number of the sub-assembly.

Example: V04 in the circuit diagram 'mixer 1' ≅ V3304
 L01 in the circuit diagram 'oscillator 2' ≅ L2501

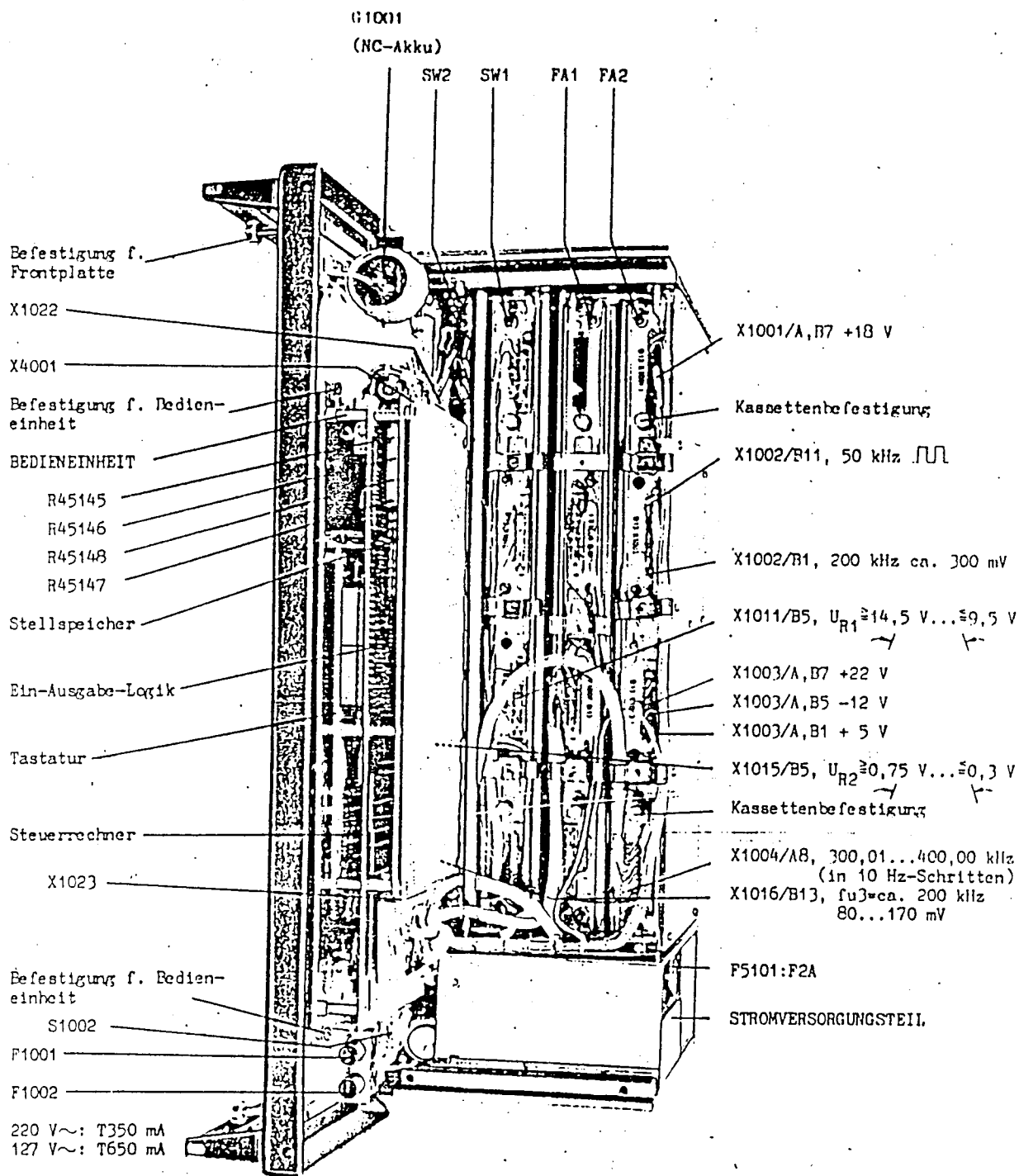
When ordering spare parts, these four-(five)- digit numbers are to be indicated.

- Marking of subassemblies in printed circuits:

Code No.	Subassembly/printed circuit	Drwg.-No.	
00	Casing	1340.042-01001	
	DC filter	1340.042-01022	
10	<u>Plug-in</u>	1340.041-00001	
20	<u>Frequency processing</u>)	1340.041-01211	
21	Oscillator 1	1340.037-01251	
22	Frequency divider 1	1340.037-01252	
23	Oscillator 3	1340.039-01253	
205	<u>Frequency processing</u>)	1340.041-01221	
24	Reference frequency	1340.037-01254	
25	Oscillator 2	1340.037-01255	
26	Frequency divider 2	1340.037-01256	
28	F1 demodulator	1340.041-01258	
30	<u>Signal path 1</u>)	1340.041-01311	(EKD 511)
		1340.041-01312	(EKD 512)
31	Preselector 1	1340.037-01351	
32	Preselector 2	1340.041-01352	
33	Mixer 1	1340.041-01353	
34	Mixer 2	1340.041-01354	
305	<u>Signal path 2</u>)	1340.041-01321	(EKD 511)
		1340.041-01322	(EKD 512)
35	Carrier oscillator	1340.037-01355	
36	IF2/B	1340.041-01356	(EKD 511)
		1340.041-01366	(EKD 512)
37	IF2/A	1340.041-01357	(EKD 511)
		1340.041-01367	(EKD 512)
38	Demodulator and AF section	1340.039-01358	
40	<u>Control unit</u>)	1340.041-01401	
41	Diode board	1340.041-01451	
42	Transistor board	1340.041-01452	
43	Input-output logic	1340.041-01453	
44	Control computer	1340.041-01454	
45	Register and interface	1340.041-01455	
46	Display	1340.041-01456	
47	Keyboard, complete	1340.041-01402	
50	<u>Power supply section</u>)	1340.039-01500	
51	Transverter	1340.039-01551	

*) Spare subassemblies according to spare part list E7

static
Hauptung cover
* wird verlegt



86-029a

Figure 1
Plug-in with the front plate swung down

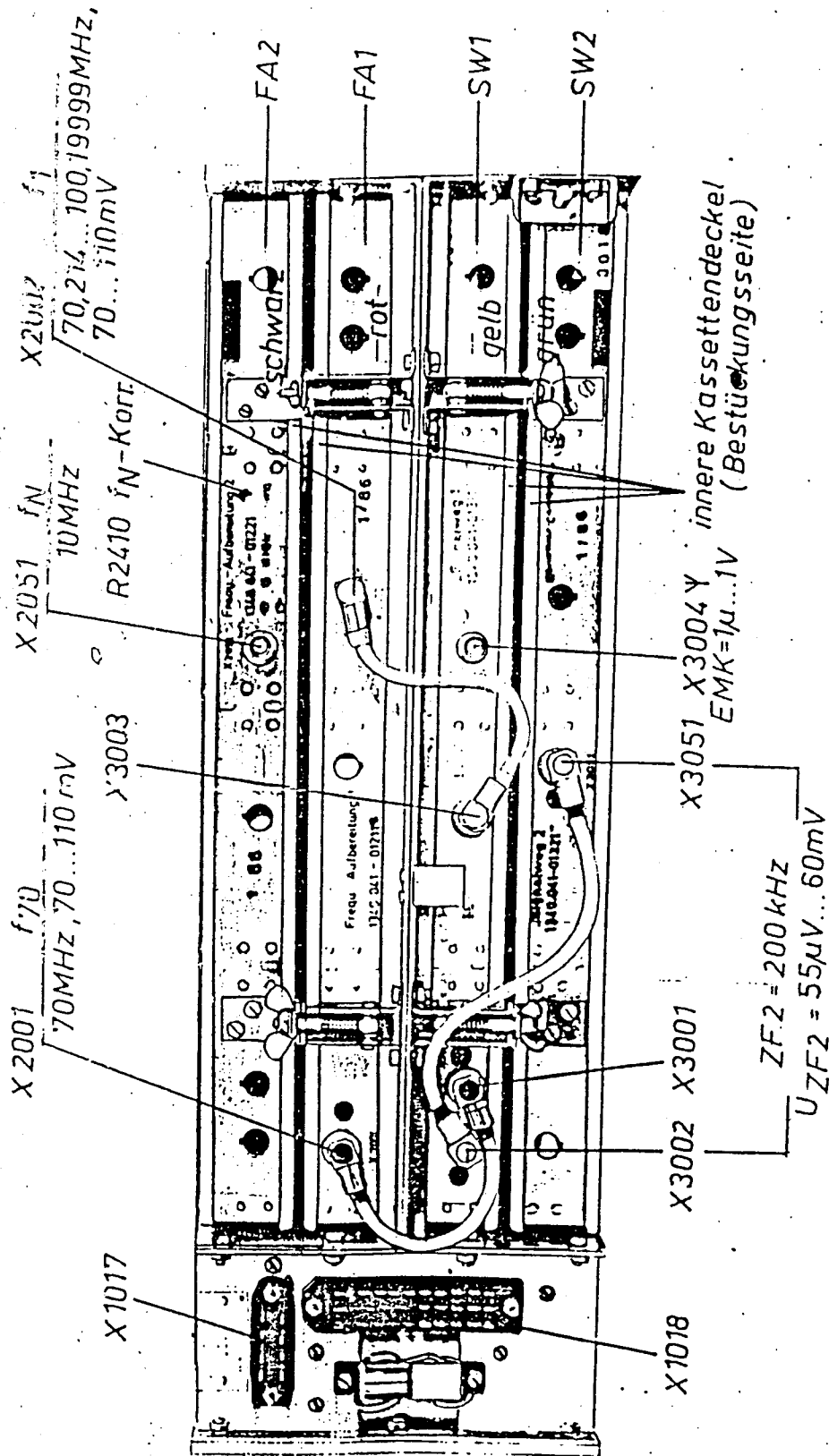


Figure 2
 Plug-in - Rear view

the functionability of the receiver by subassembly exchange

To make service work easier and to reduce the outage times of the receiver, we recommend to replace entire subassemblies. For this purpose, the manufacturer of the equipment offers spare subassemblies according to the spare part list E7.

Variant	EKD 511	EKD 512
Spare subassembly	1340.042-01871 E7	1340.042-01872 E7
Frequency processing 1	1340.041-01211	1340.041-01211
Frequency processing 2	1340.041-01221	1340.041-01221
Signal path 1	1340.041-01311	1340.041-01312
Signal path 2	1340.041-01321	1340.041-01322
Control unit	1340.041-01401	1340.041-01401
Power supply section	1340.039-01500	1340.039-01500

Attention!

The cassettes of receiver EKD 500 and of EKD 300 are not interchangeable.

The Power supply sections of receiver EKD 500 and EKD 300 can be exchanged with each other.

Subassembly exchange requires no readjustment for the functionability of the receiver.

Sections 6.1. to 6.5. contain hints on readjustment in order to minimize tolerances.

In case that the fault symptoms detected during functional check (carried out in accordance with Section III/5) did not result in localization of the faulty subassembly, checks on the receiver plug-in outside the casing are necessary.

- . Attention! Pull mains plug before taking the plug-in out of the casing.
- . Establish electric connections between casing and plug-in via the 30-core adapter cable (contained in the accessories). For checks via interfaces EXT and EXP, connect additionally the 8-core adapter cable.
- . Dismounting and mounting according to Section 3.
- . For all checks mentioned in Section 5 opening the cassette lids is not necessary.

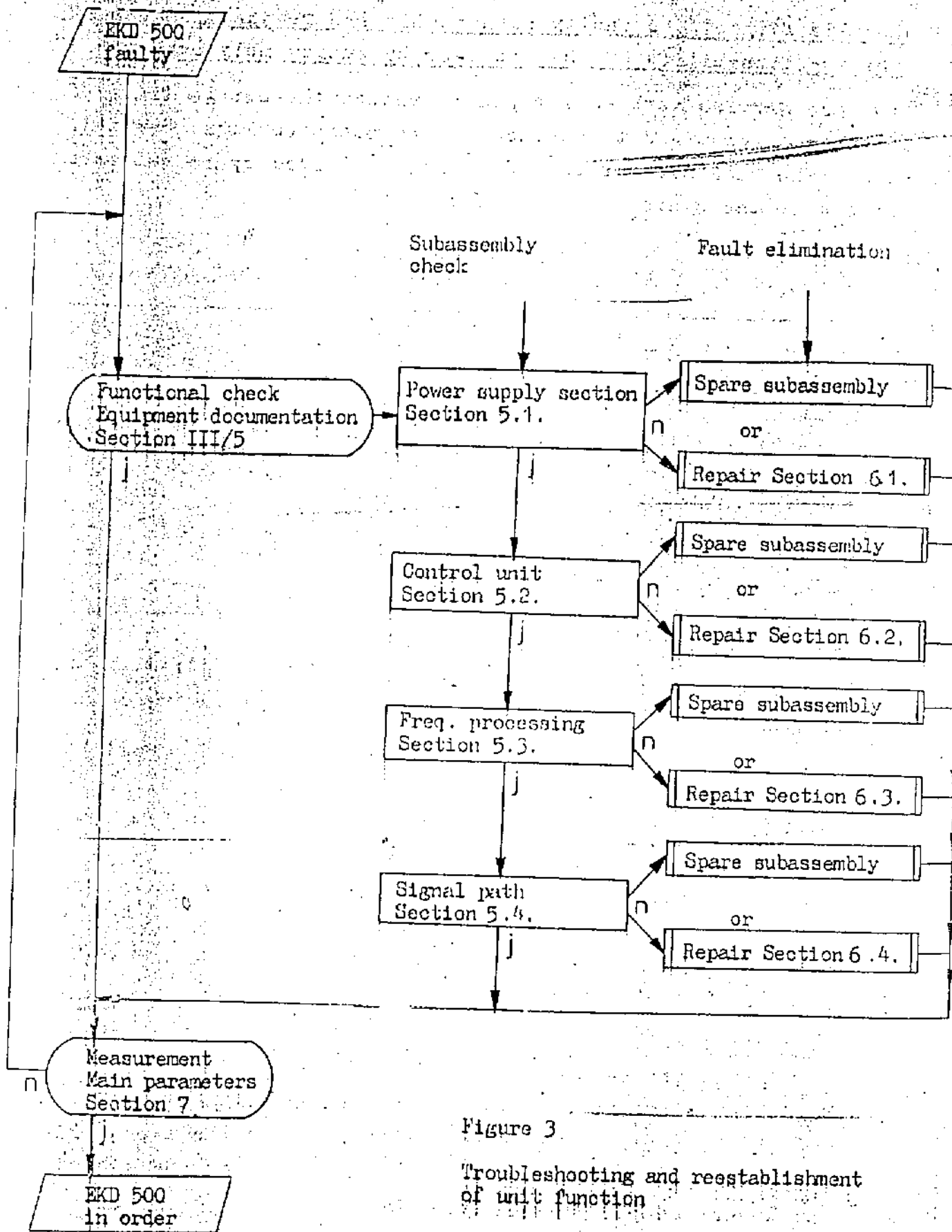


Figure 3

Troubleshooting and reestablishment
of unit function

The undermentioned remarks serve to detect the faulty subassembly with only a few test means.

1. Check 'power supply section'

5.1.1. Measuring of the output voltages with digital voltmeter (P9)

	Test point	Correction with
+18 V \pm 0.2 V	X1001/A7, B7	R 5213
+ 5 V \pm 0.1 V	X1003/A1, B1	R 5217
+22 V \pm 2 V	X1003/A7, B7	-
-12 V \pm 0.1 V	X1003/A5, B5	R 5114

5.1.2. In case of voltage breakdowns

+18 V, +5 V, +22V, -12 V: F 1001 and F 1002

+18 V, +5 V, +22V: F 5101

For battery operation: battery cable
fuse

} to be
checked

For localizing short-circuits in the subassemblies, the cassettes are to be withdrawn one after the other.

5.1.3. In case of faulty power supply section

→ replacement by spare part subassembly
(Pay attention to the correct voltage adjustment
(X 5002) or

→ repair according to Section 6.1.

5.2. Check 'control unit'

5.2.1. When the functional check of the receiver (equipment documentation Section III/5) proved the control unit being faulty

- . fault recognition by control test A1 to A5
- . no correspondence between operation and display

the following has to be carried out:

- replacement by spare subassembly
(required readjustment: tolerance minimization for receiving level display;
balance R 45145, R 45146, R 45148, R 45147 according to Section 6.2.) or
- repair in accordance with Section 6.2.

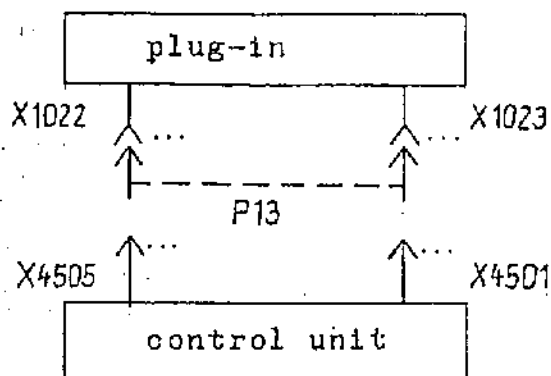
5.2.2. Functional breakdown of the receiver although operation and display correspond with each other

- Possible fault reasons:

- . Register and interface - output faulty
- . Frequency processing faulty
- . Signal path faulty

- Fault delimitation by substitution of the control unit by test plug pair P 13

— (Drwg.-No. 1340.042-01602)




- The test result supplies other hints on possible fault sources: 'control unit'

- 'frequency processing1' and '2'
- 'signal path 1' and '2'

unscrew front plate fastening and swing front plate down by 90°.

Separate terminal sockets X 1022 and X 1023 from the control unit and connect them with test plug pair P 13.

Changeover switch at P 13 to position  according to EKD adjustment


13 E	0.00
------	------

 GC 1, SEL 0
i.e.: PLL2: $f_2/100 = 400 \text{ kHz}$
PLL3: $f_3 = 69.6 \text{ MHz}$
 $\pm f_70$

If: A1 tone audible in the loudspeaker, at the IF output (X 0003): 200.000 kHz (measure with P1),

Then: frequency processing 1: }
frequency processing 2: } troublefree
signal path 1 (from mixer 1): }
signal path 2: }
register and interface output: } faulty
(incl. connection cables)

- Replace control unit by spare subassembly (required readjustment: tolerance minimization for receive level display according to Section 6.2.)
- or repair in accordance with Section 6.2.

Changeover switch at P 13 to position  according to EKD adjustment

13 E	9999.99
------	---------

 GC 1, SEL 0
i.e.: PLL2: $f_2/100 = 300.01 \text{ kHz}$
PLL3: $f_3 = 69.69999 \text{ MHz}$
 $\pm \Delta f_70$

Connect X 2051 ($f_N = 10 \text{ MHz}$) with receiver input (X 0001) by means of RF cable 1340.037-01124 (in the accessories).

If: A1 tone audible in the loudspeaker, at the IF output (X 0003): 199.99 kHz (measure with P1),

Then: frequency processing 1: }
frequency processing 2: } troublefree
signal path 1: }
signal path 2: }

register and interface output: faulty
(incl. connection cables)

- Replace control unit by spare subassembly
(required readjustment: receive level display
according to Section 6.2.)
- or repair in accordance with Section 6.2.

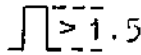
5.3. Check 'frequency processing'

5.3.1. Cassette 'frequency processing 2'

- f2/100 to X 1004/A 8 (frequency divider 2)

. Check of frequency (with P1) and voltage

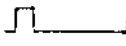
(with P6)

f_E input (kHz)	f2/100 (kHz)	$u_{f2/100}$ (V_{SS})
0.00	400.00	 ≥ 1.5
99.99	300.01	

. Potential conversion of all logic conditions for 'frequency divider 2' drive.

f_D input (kHz)	f2/100 (kHz)
77.77	322.23
88.88	311.12

- 200 kHz at X 1002/B 11 (reference frequency)
 check of frequency: 200.000 kHz (with P1)
 and voltage: 150 mV to 300 mV (with P2)

- 50 kHz at X 1002/B 1 (reference frequency)
 check of frequency: 50.000 kHz (with P1)
 and voltage:  $\geq 2.4 V_{SS}$ (with P6)

- In case of faulty 'frequency processing 2':
 → replacement by spare subassembly
 → or repair in accordance with Section 6.3.

5.3.2. Cassette 'frequency processing 1'

- f1 to X 2002 (rear of the plug-in)

. Check of frequency (with P1) and voltage (with P2) for the subranges of oscillator 1

range of osc. 1	f_D input (kHz)	f1 (kHz)	admissible fault Δf (Hz)	u_{f1} across 50 ohm (mV)
1a	0.00 1999.00	70200.00 72199.00	} $\cong \pm 150$ *)	} 80 ... 100
1b	2000.00 9999.00	72200.00 80199.00		
2	10000.00 29999.00	80200.00 100199.00		

Check of f1 with potential conversion of all logic conditions for the drive of 'frequency divider 1'

f _E input (kHz)	f1 (kHz)	admissible fault Δ f1 (Hz)
17700.00	87900.00	} ≅ ± 150 *
28800.00	99000.00	

* Δ f1 = Δ f70 ≅ 150 Hz
 Δ f70 is eliminated with the 2nd frequency conversion (mixer 2)

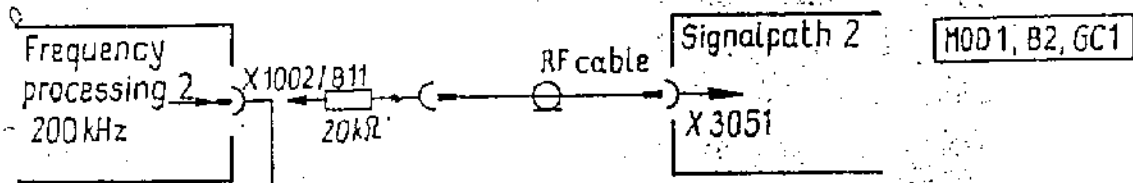
- f 70 to X 2001 (rear of the plug-in)
 Check of frequency (with P1) and voltage (with P2)

f70	70 MHz ± ≅ 150 Hz
u _{f70}	80 mV to 100 mV

- In case of faulty 'frequency processing 1':
 - replacement by spare subassembly
 - or repair in accordance with Section 6.3.

Precondition: 'power supply section' } troublefree
 'control unit' }
 'frequency processing' }

5.4.1. Check 'signal path 2' with 200 kHz from 'frequency processing 2'

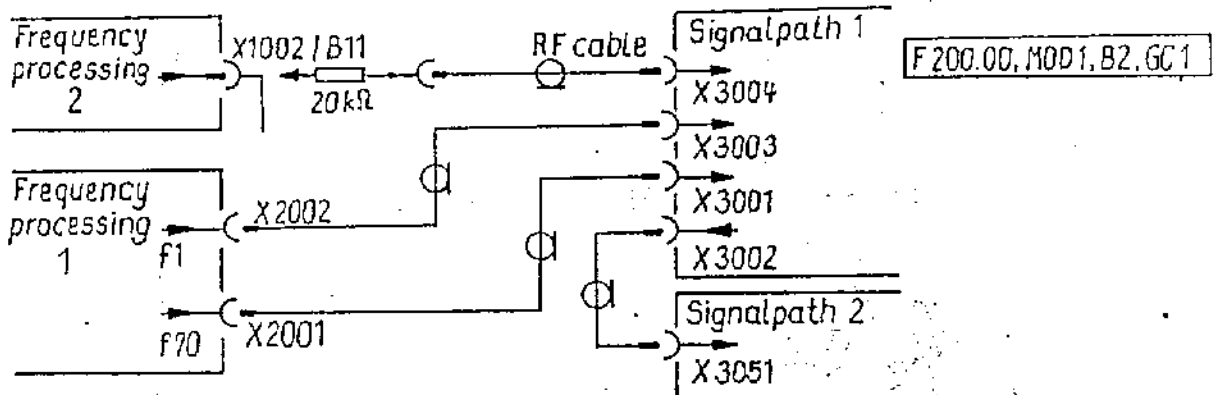


- 'signal path 2' in order: E_γ display .. LED row: 80 to 100 dB (μV)
 digital: 42 ... 52
 A1 tone available

- 'signal path 2' faulty:

- replace it by spare subassembly
 (readjustment: tolerance minimization for E_γ display according to Section 6.2.)
- or repair in accordance with Section 6.4.

5.4.2. Check 'signal path 1' and '2' with 200 kHz from 'frequency processing 2'



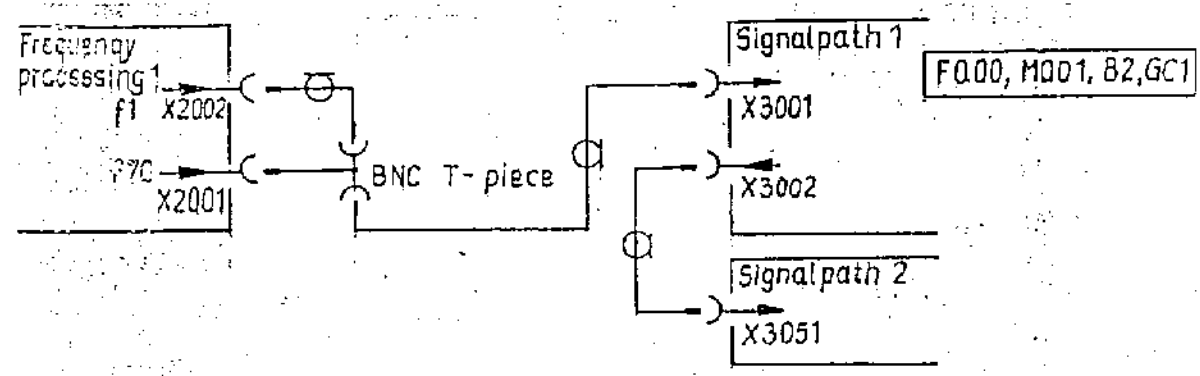
- 'signal path 1' and '2' in order:
 E_γ display: .. LED row: approx. 60 dB (μV)
 digital: 28 ... 35

A1 tone available

- 'signal path 1' faulty:
- replacement by spare subassembly
(readjustment: tolerance minimization for E_y display according to Section 6.2.)
- or repair in accordance with Section 6.4.

5.4.3. Check 'signal path 1 - subsections'

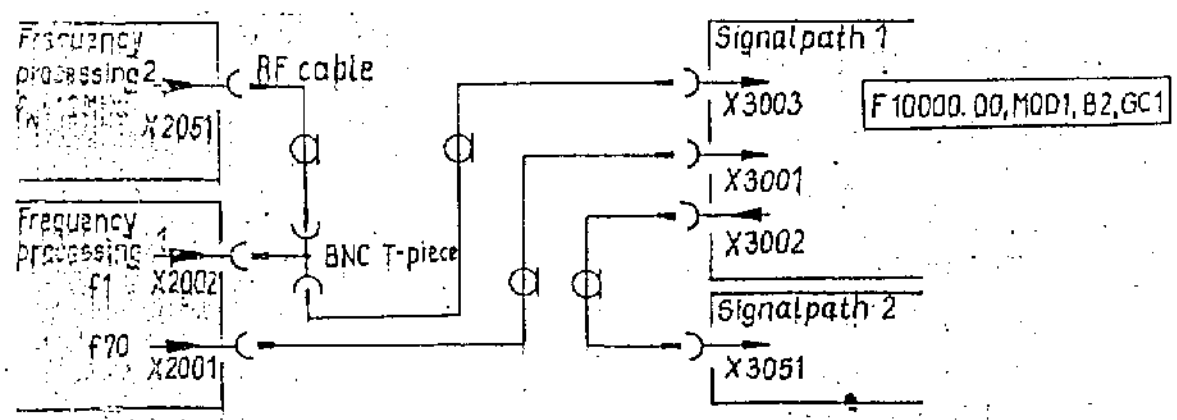
5.4.3.1. Mixer → X 3002 → signal path 2



- Signal path 1 - subsections in order:
- E_y display . LBD row: 80 ... 90 dB (μV)
- . digital: 38 ... 45
- A1 tone available

- Signal path 1 - subsections F70 ampl. → mixer 2 → X 3002: faulty
- replace signal path 1 by spare subassembly
(readjustment: tolerance minimization for E_y display according to 6.2.)
- or repair in accordance with Section 6.4.

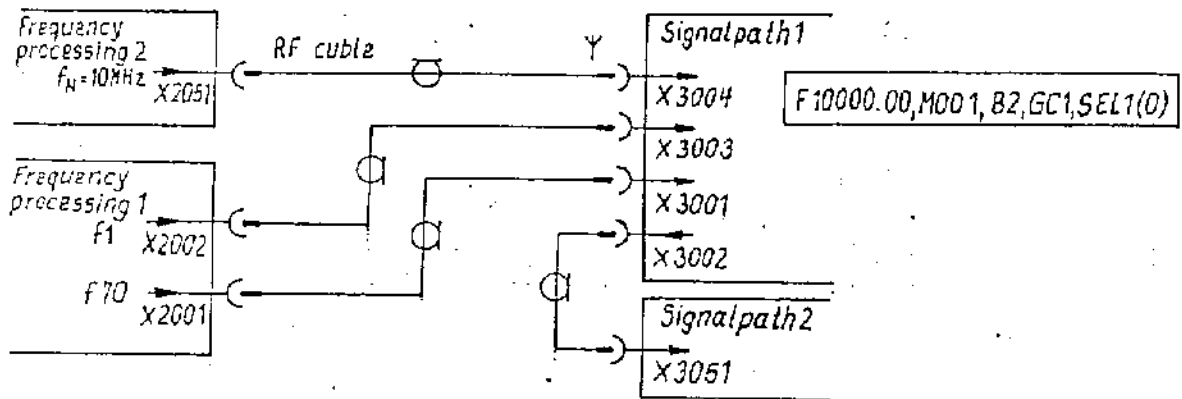
5.4.3.2. Mixer → IF-1 ampl. → Mixer 2 → X 3002 → signal path 2



- Signal path 1 - subsection in order:
 E_{γ} display . LED row: approx. 90 dB (μ V)
 . digital: 42 ... 48
 A1 tone available

- Signal path 1 - subsection: f1 ampl. —> mixer 1 —>
 OF1 ampl —> 70.2 MHz crystal filter: faulty
 —> replace signal path 1 by spare subassembly
 (readjustment: tolerance minimization for
 E_{γ} display according to Section 6.2.)
 —> or repair in accordance with Section 6.4.

- 5.4.3.3. Preselector 1 and 2 —> control element 1 —> mixer 1 —>
 IF1 ampl. —> mixer 2 —> X 3002 —> signal path 2



- Signal path 1 in order:
 E_{γ} display . LED row: approx. 100 dB (μ V)
 . digital: 47 ... 53
 A1 tone available
- Signal path 1 - subsection:
 X 3004 —> preselector 1 and 2 —> control element —>
 —> TP = 30 MHz: faulty
 —> Replace signal path 1 by spare subassembly
 (readjustment: tolerance minimization
 for E_{γ} display according to 6.2.)
 —> or repair in accordance with Section 6.4.

6. Repair of the faulty subassembly

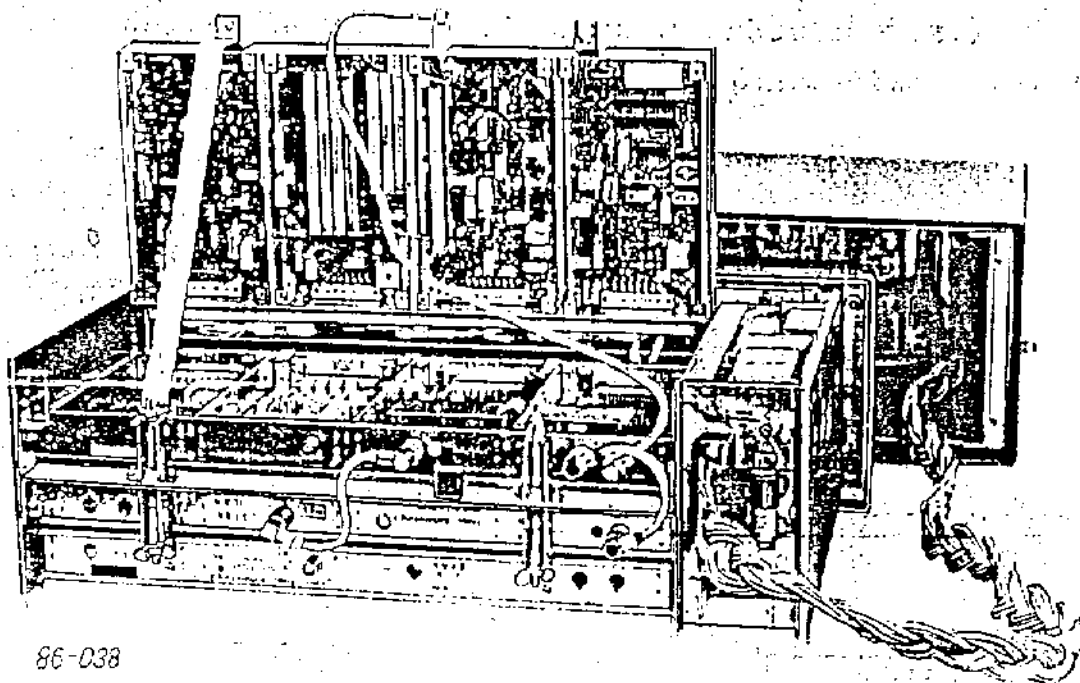


Figure 4

Service work on the cassettes of the signal path (SW1 and SW2) or on the cassettes of the frequency processing (FA1 and FA2)

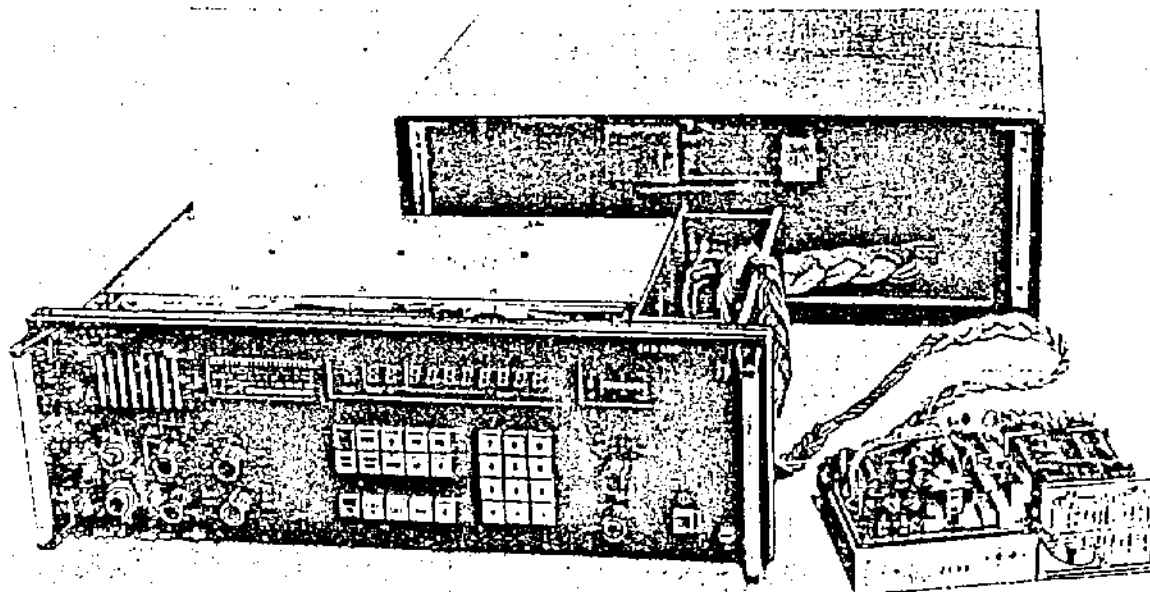


Figure 5

Unit arrangement for service work on the power supply section

Master Library
Digitized by
USG Center
for
Intelligence

Approved for
Public Release

6.1. Power supply section 1340.039-01500

6.1.1. Input and output values

EKD: $f_E = 2.00 \text{ kHz}$

B_{RB} , channel A

medium volume, $I_{\square} = 40 \text{ mA}$

Power consumption of the entire unit

Current measurements with PB at U_{rated} in the mains- or battery lead.

All indicated current values are approximate ones.

Mains operation: $\sim 127 \text{ V ac}$: approx. 400 mA
 $\sim 220 \text{ V ac}$: approx. 230 mA

Battery operation: $= 24 \text{ V dc}$: approx. 1.5 A
 $= 12 \text{ V dc}$: approx. 3.0 A

Output voltages

For measuring or correction:

Operate the plug-in outside the casing via the 30-core adapter cable (accessories).

Measurement with P6 at the measuring points according to Figure 1

+18 V : at X1001/A7, B7

+22 V : at X1003/A7, B7

-12 V : at X1003/A5, B5

+5 V : at X1004/A1, A2

Line corrections only after an operating time of the receiver of = 30 min.

+18 V \pm 100 mV correction with R 5213 (I = approx. 650 mA)

+5 V \pm 20 mV correction with R 5217 (I = approx. 1.2 A)

-12 V \pm 50 mV correction with R 5114 (I = approx. 250 mA)

+22 V - 2 V - - (I = approx. 70 mA)

Check current load before every correction.

Hum voltages of the output voltages

The ripple is to be measured with load and 220 V ac input voltage by means of P6 (peak-to-peak value).

- +18 V path : \approx 30 mV (20 kHz)
- +5 V path : \approx 50 mV (20 kHz)
- 12 V path : \approx 20 mV (100 Hz or noise)
- 22 V path : \approx 50 mV (20 kHz + 100 Hz)

Centro. behaviour

With change of the input voltage by $\pm 10\%$, the variations of the individual output voltages - measured with P9, amount to:

- +18 V path : $\Delta U = 60$ mV
- +5 V path : $\Delta U = 20$ mV
- 12 V path : $\Delta U = 10$ mV

The input voltage variation is to be simulated with the adjustable transformer (P 12).

6.1.2. Measuring values within the power supply divider

measured with mains operation 220 V and load

Rectifier voltages

- +18/+5 V path
(measured at C 5903) : approx. 30 V
- 12 V path
(measured at C 5105) : approx. 20 V
- Additional voltage for 22 V path
(measured at C 5108) : approx. 4 V

Overcurrent limitation

The +18 V-, +5 V-, and -12 V path are provided each with a permanently adjusted current limitation.

This current limitation is to be checked by an additional load (slide resistor (R1) 100 \rightarrow 0 ohm).

Path	Sweep current	s-o current
+18 V path	approx. 2 A	≅ 2.5 A
+5 V path	approx. 3 A	≅ 4 A
-12 V path	approx. 0.4 A	≅ 0.25 A

Shorting the +18 V- and +5 V paths causes switching controller noises in the audible range.

Curve shape

At the test points P01 to P06 indicated in the circuit diagram the prescribed curve shapes shall be detected with P6.

Working frequency

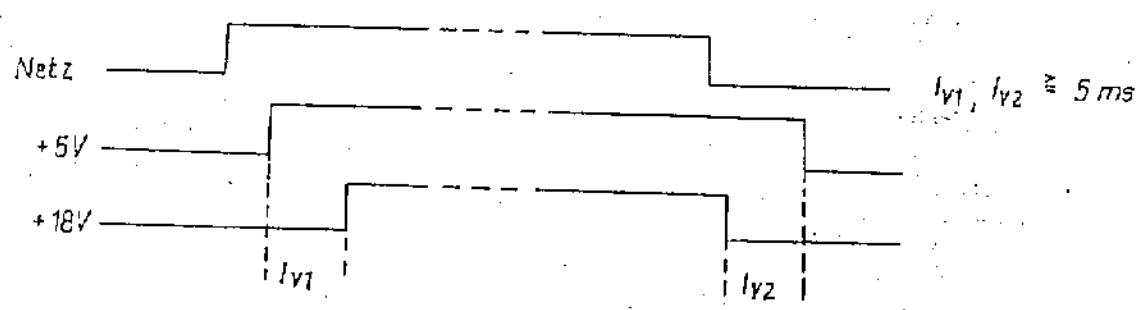
The transverter operates at rated voltage with a frequency of roughly 80 Hz.

It greatly depends on the input voltage.

The switching controller is to be adjusted to 20 kHz \pm 3 kHz by means of R 5227.

Closing behaviour

The unit-specific time sequence of the partial voltages in case of ON and OFF switching is the precondition for the functionality of the control unit.



t_{y1}, t_{y2} = delay time of ON and OFF switching

When t_{y1}, t_{y2} is not kept, the power supply needs repair.

26

6.1.3. Troubleshooting table

Fault	Possible fault reason	Fault elimination
<p>a) Transverter does not start to oscillate</p>	<ul style="list-style-type: none"> - False voltage protection responds - V5101, V5102 faulty - Contact troubles at K5001/5002 - Contact troubles at circuit closer on front plate - Overload at secondary end 	<ul style="list-style-type: none"> - viz. b) - Replace V5101, V5102 - Replace K5001, K5002 - viz. c) - causes increased power consumption with mains operation.
<p>b) False voltage protection responds</p>	<ul style="list-style-type: none"> - Battery voltage does not comply with the voltage adjusted on the terminal board X 5002. - Component in the protective circuit faulty 	<ul style="list-style-type: none"> e.g. V 5107, V 5106, V 5103, K 5101
<p>c) Starting aid for oscillation not excited (C 5101 not charged or not discharged with connection or disconnection)</p>	<ul style="list-style-type: none"> - Interruption in the oscillation-start circuit X 5001/b3(+)- k 02/7/5/11/13- R 5111-V 5110- circuit closer (on front plate) 	

Fault	Possible fault reason	Fault elimination
d) F 5101 responds	<ul style="list-style-type: none"> - Overvoltage in the +5 V- or +18 V path - Short in the circuit 	<ul style="list-style-type: none"> - Disconnect load in the unit (e.g. TTL-circuits) - desolder connections 6 and 7 on pc board 51 - check if an exceeding voltage presents at the output of one of the two paths. In this case e.g. transistor V 5101 or V 5102 or the control (MAA 723) is faulty. - Separate load and check if the fuses keep responding. In this case e.g. V 5212, V 5214 or transistor insulation faulty.
	<ul style="list-style-type: none"> - Overvoltage protection circuit faulty 	<ul style="list-style-type: none"> - e.g. V 5107, V 5108 or V 5109 (thyristor)
e) Noise caused by switching controller	<ul style="list-style-type: none"> - Sawtooth generator (V 5210, V 5207) faulty 	<ul style="list-style-type: none"> - Check curve shapes at P 01, P 02. Trace signal up to circuit connection 3

Fault	Possible fault reason	Fault elimination
c) Output voltage of the -12-V-path too high	<ul style="list-style-type: none"> - V 5001 faulty - N 5101 faulty 	
d) Frequency of rectifier hum voltage amounts, with mains oper., to 50 Hz instead of 100 Hz	<ul style="list-style-type: none"> - One rectifier branch of the respective rectifier faulty 	<ul style="list-style-type: none"> - Measurement at C 5105: -12-V path C 5108: Additional voltage for 22-V path C 5003: +5-V path +18-V path

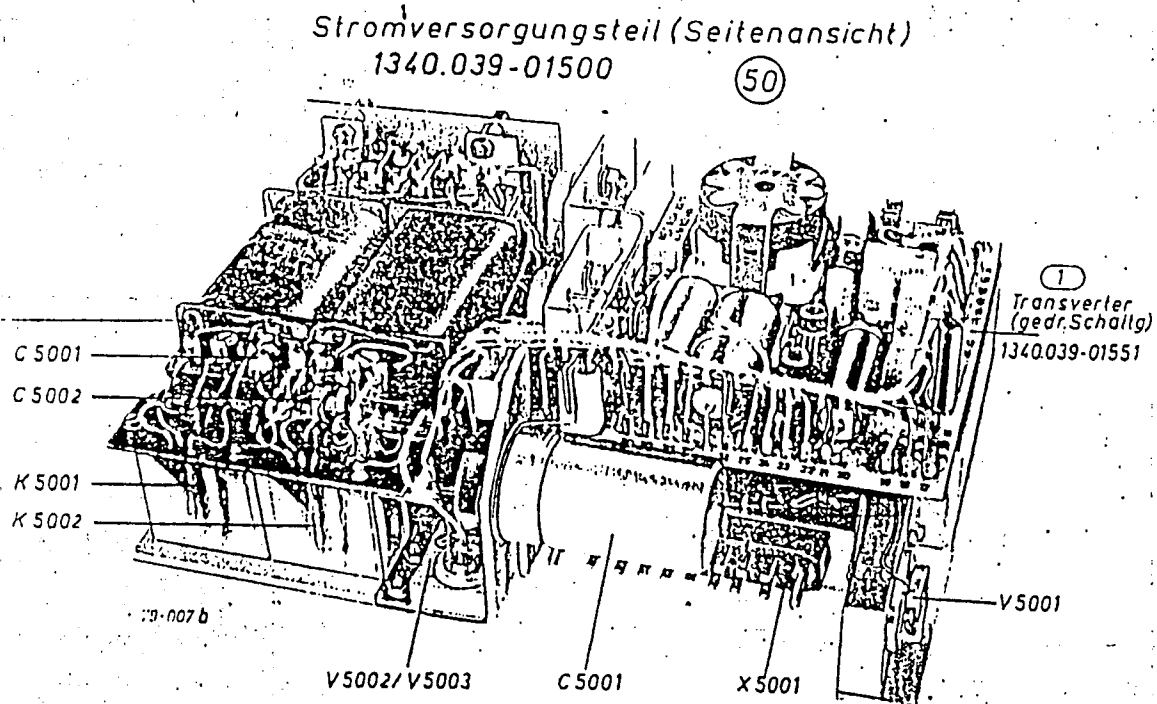


Figure 6
Power supply section 1340.039-01500

Stromversorgungsteil (Seitenansicht)
1340.039-01500

(50)

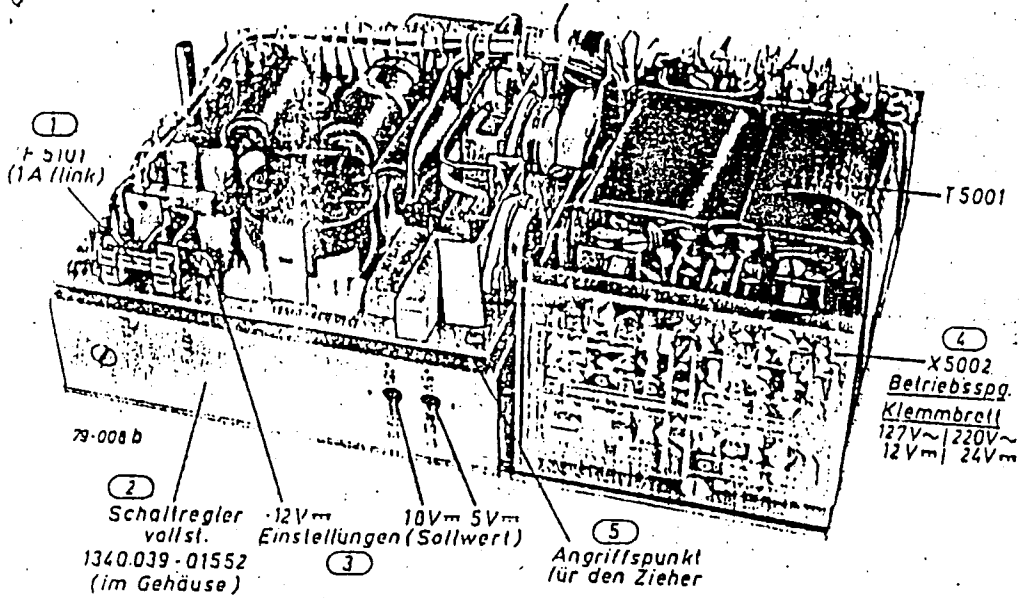


Figure 7

Power supply section 1340.039-01500

6.2. Control unit

6.2.1. Function principle

After switching on the unit as well as after mains failure the microcomputer is brought in the initial position and the receiver is adjusted to its condition before the disconnection or mains failure.

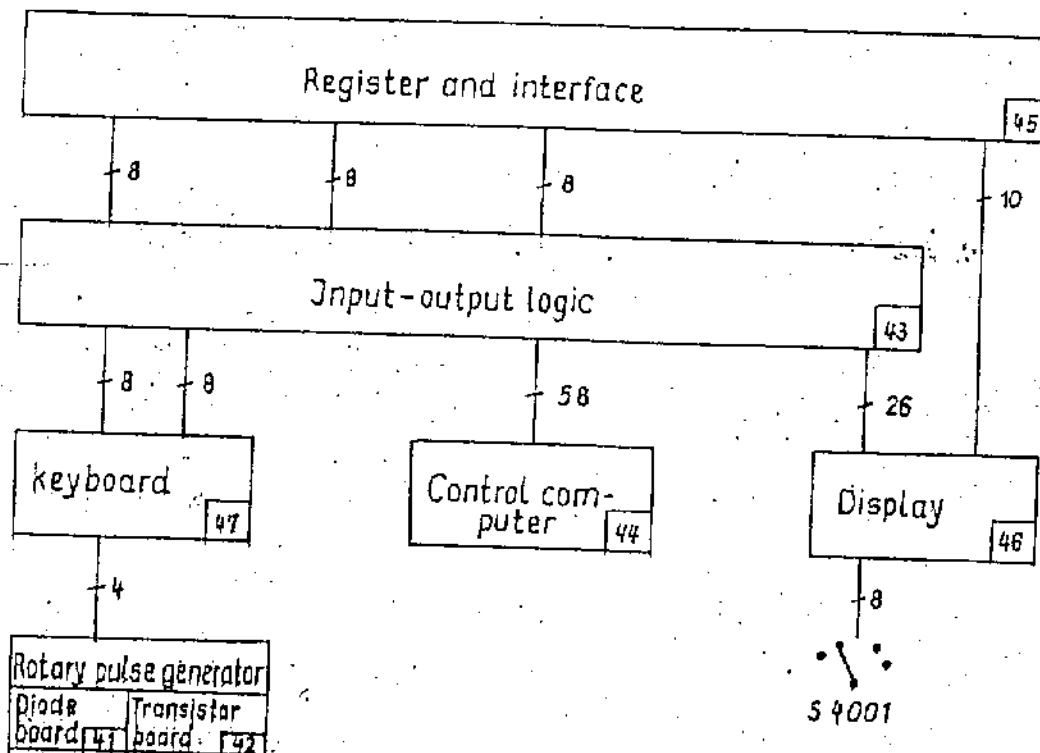
Subsequently, a program for multiplexer control of the display is initiated.

All operating measurements carried out via keyboard or 24-V interface cause via port A an interruption of the PIO circuit.

Mains failure and test routines are controlled via the non-maskable interrupt input of CPU. The RAM circuits of the control computer are backed by an internal battery.

In case of a total breakdown, it is recommended to start troubleshooting in the computer core because fault detecting is supported by the software. The following sequence is to be adhered to:

Control computer - input-output logic - keyboard - display - register and interface.



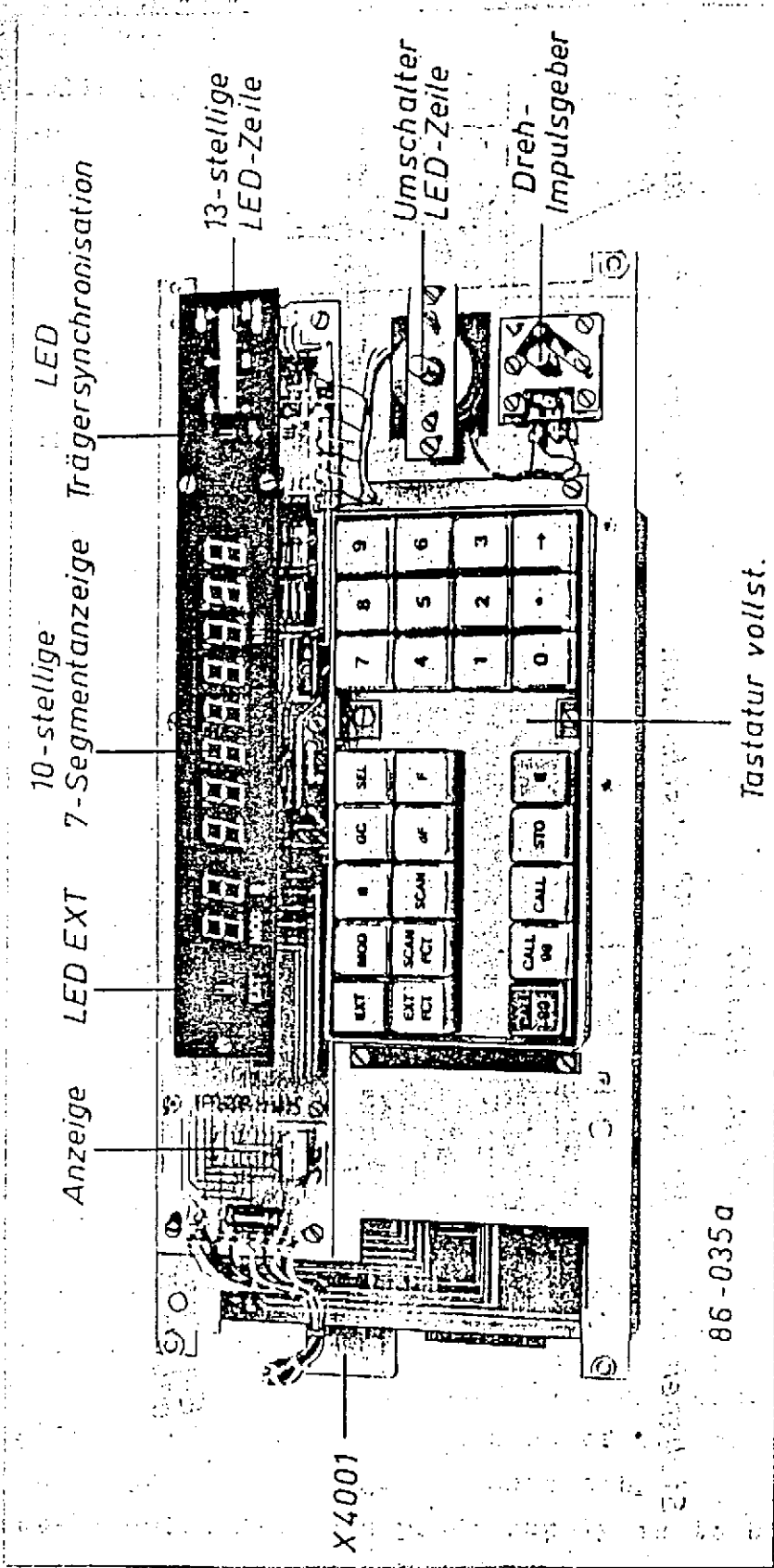


Figure 8 Control unit Front view

86-035a

35

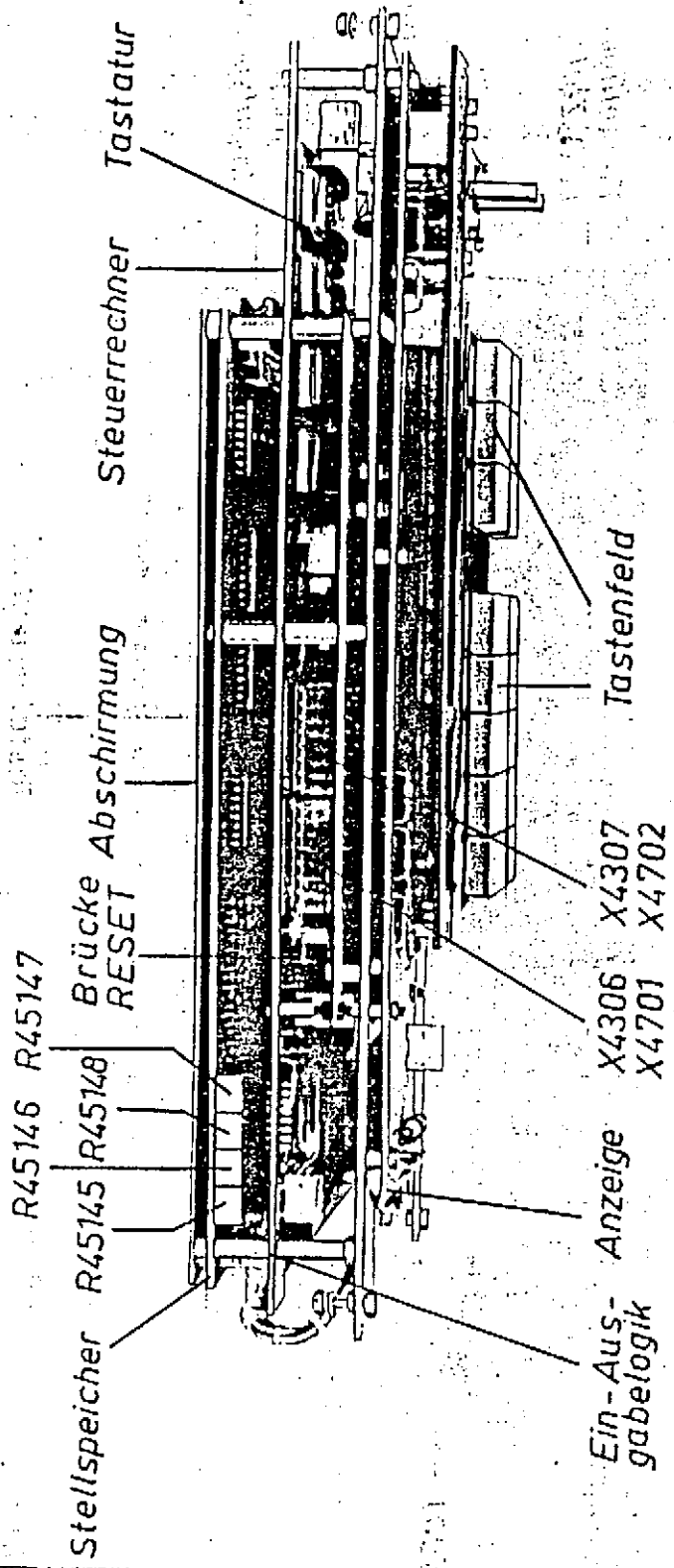


Figure 9
Control unit - view from above

86 - 036 a

Wenn Eigentum
Militär ist
es wird zerstört

6.2.2. Test and check arrangements

- Control unit inserted

The following components of the plug-in are accessible from above:

- R45145 ... R45147 to balance the control voltage linearization (cf. Section 6.2.9.)
- X4701, X4702 to check and repair the keyboard (cf. Section 6.2.7.)
- Strip 01-02 (RESET) on input-output logic.

Open the receiver front plate, remove screening. The control unit is accessible from the soldering side of the register and interface.

On the soldering side of the control computer U_{RAM} can be checked at CA408.

- Control unit removed

By means of connection adapter P15 the control unit can be operated from an external mains unit; +5 V, +18 V, -12 V, \perp

- Check of display and keyboard

Open the front plate of the plug-in, slacken the plug-and-socket connections X4501-X1023 and X4505-X1022, take off the control unit and place it upright such that the plug-and-socket connections can be reestablished again. The complementation side of the display is accessible. If necessary, unscrew the cover.

- Check of control computer and input-output logic

Take off the control computer; establish connection plug-in X1023 - input-output logic X4303/04/05 by means of adapter cable P14. The complementation side of the control computer and the input-output logic is accessible.

Connect P14 with P15 when power supply is to be performed from an external mains unit.

6.2.3. Repair sequence 'local operation'

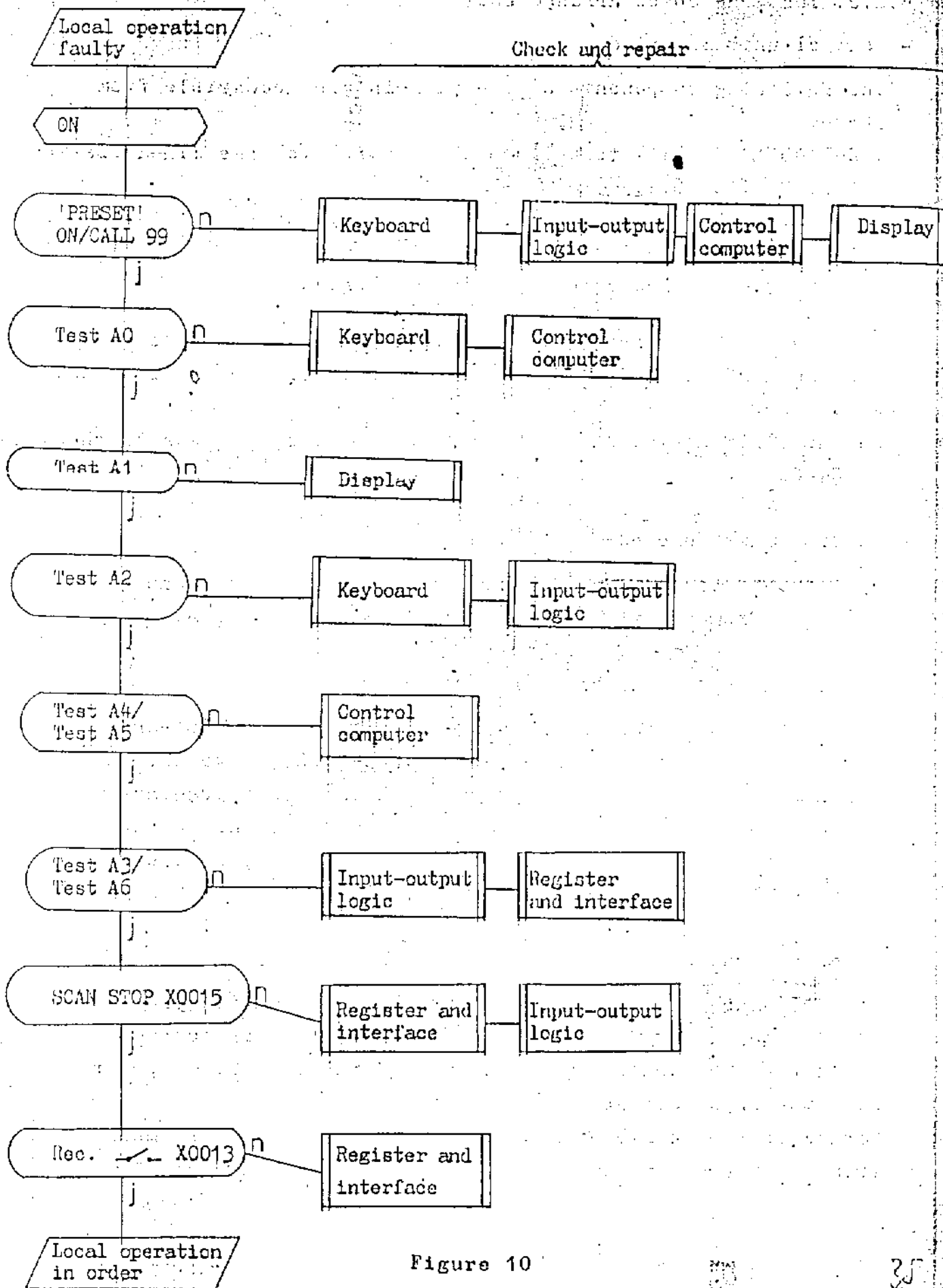


Figure 10

35

6.2.4. Repair sequence Operation 'external'

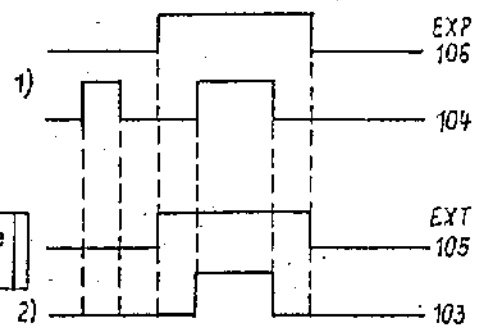
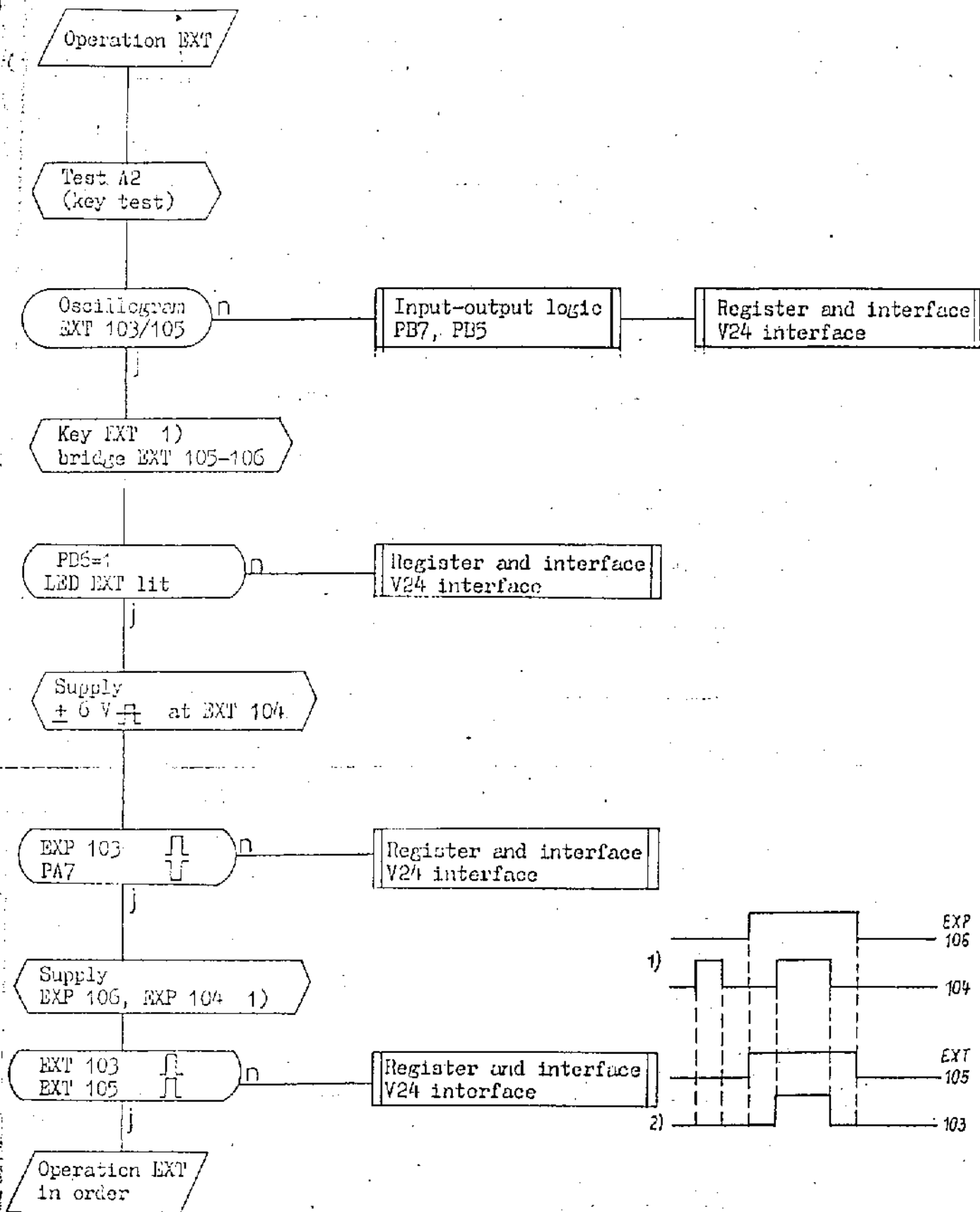


Figure 11

1) The unit is to be programmed in advance as 'slave'.

39

6.2.5. Control computer

- Operating voltages

+5 V at D04/11, U_{RAM} at C08 (cf. Section 6.2.6. U_{RAM} changeover)

- Input signals of CPU

\overline{BUSRQ} , \overline{WAIT} , \overline{RESET} , \overline{NMI} , $\overline{INT} = 1$ (≈ 3.5 V)

Clock at D04/6 $\square\square$ 1.2 MHz $U_{high} \approx 4.8$ V, $U_{low} \approx 0.5$ V

- CPU bus and store selection signals

Open wire strap 03-04, establish connection 04-13.

Cyclic program call is performed. The data bus, the address bus and the control bus of the CPU can be oscillographically checked concerning correct low-high signal change. With this, also the connections of the bus lines to the circuits as well as shorts can be checked.

Signal	U_{low}	U_{high}
D0 ... D7	} < 0.7 V	3.5 V
A0 ... A3		> 3.5 V
A4 ... A15		> 2.5 V
M1, RD, WR, MREQ, RFSH		> 2.5 V
CS0 test point 03		> 2.5 V
CS1 R07		> 3.5 V
CS2 test point 05		> 2.5 V
CS3 test point 07		> 2.5 V
CS4 test point 09		> 2.5 V
CS5 test point 11		> 2.5 V

- Software-aided checks

(cf. equipment documentation Section III/5.2.)

a. Test (key EXT and EXT PCT)

This test, an NMI access to the CPU, checks the function of the input gate PIO port A, i.e. it is tested if the data are read. Furthermore, the function of the EPROMs are checked, i.e. if data are put out.

Troublefree function:

All keys are open (PA 6...PA 0 = 78 H), serial input in STOP condition (PA 7 = 1). All EPROMs supply data.

Display: AA-A0 last receive condition. In condition AA a program loop is running cyclically. It is possible to check oscillographically the CPU signals \overline{IOMQ} , \overline{NERQ} , $\overline{M1}$, \overline{RD} , \overline{WR} , and the decoder signals CS 0 ... CS 5.

Malfunctioning:

The key code of a faulty key is indicated or PA 7 is not in STOP condition or port A of the PIO does not work.

Display 01 indicates: EPROMs by switching further with key (01, 02 ...); the faulty EPROM does not appear on the display but any display as e.g. FF. Consider the departure from the correct sequence.

b. Test A4 RAM test

Results: FF, F1, F2

FF = troublefree, F1 = RAM 1 (D 4405) faulty,
F2 = RAM 2 (D 4406) faulty.

a. Test A5 ROM test

Results: FF, F1, F2, F3, F4

FF = troublefree, F1 ... F4 = faulty EPROM D 4408 ... D 4411.

Attention

Individual EPROMs must not be exchanged.

When a component - circuits D 4408, D 4409, D 4410, D 4411, (D 4412) - has proved itself to be faulty, the entire pc board control computer 1340.041-01454 is to be replaced.

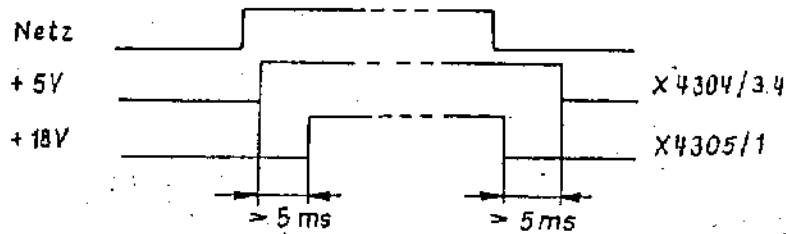
6.2.6. Input-output logic

Test sequence:

- RESET and NMI generation
- RAM changeover
- Input-output gate addresses and assigned output signals
- RESET and NMI generation

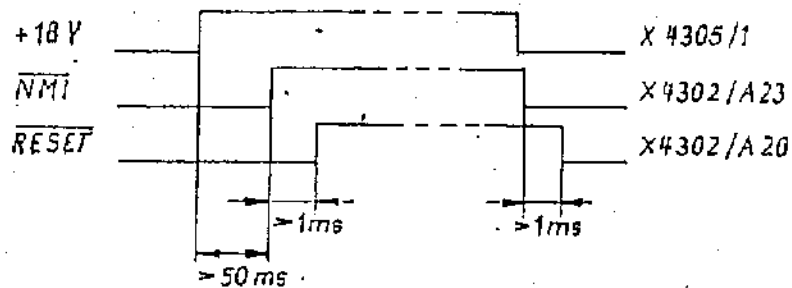
unit switch ON/OFF, check voltage curve with double-beam oscillograph P5

+5 V and +18 V

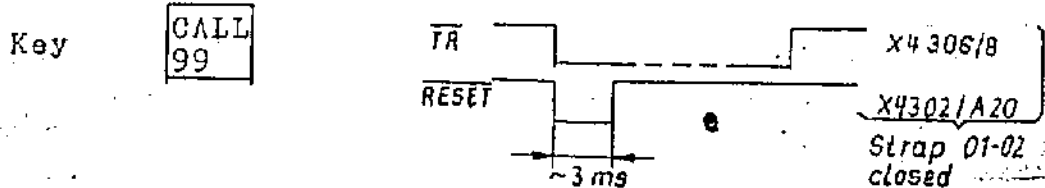


When these conditions are not met — repair power supply in accordance with Section 6.1.

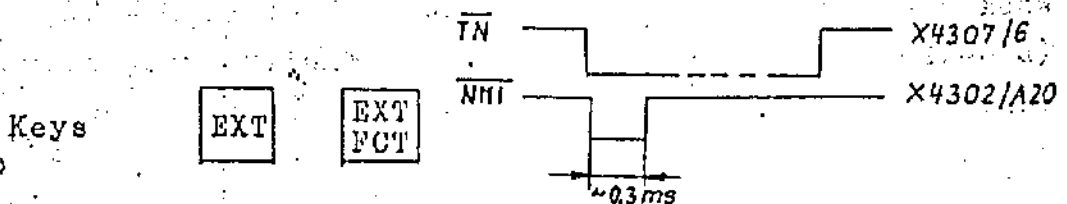
NMI and RESET



RESET pulse



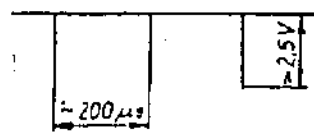
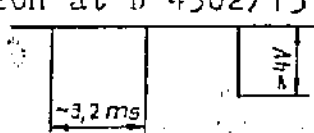
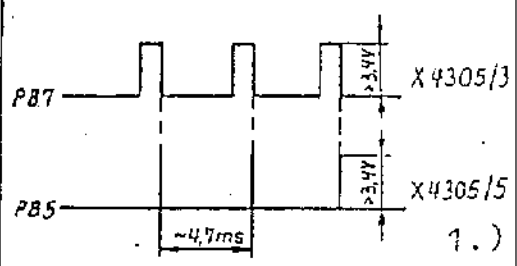
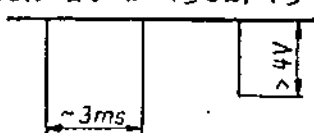
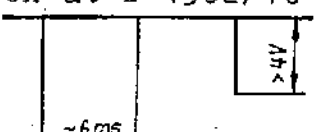
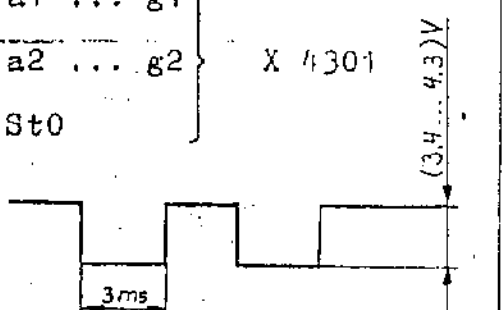
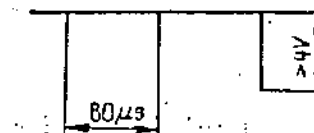
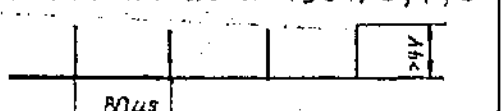
NMI pulse



- U_{RAM} changeover

Unit switch	U _{RAM} to C 4408
ON	+5 V from power supply
OFF	+ (3.6 ... 4.1)V from support battery

- Input-output gate addresses and assigned output signals

Input	Output	Pulses to be checked	Output signals
Test	AA	$\overline{30H}$ at D 4302/12 	
Test A1	8 ... 8	$\overline{10H}$ at D 4302/14 $\overline{20H}$ at D 4302/13 	a1 ... g1 a2 ... g2 p1, p2 St0 ... St4 X 4301 2.)
Test A2 Key EXT	00	$\overline{30H}$ at D 4303/12 Oscillogram without synchronization U 2.5 V	 X 4305/3 X 4305/5 1.)
Test-A3	A3 00	$\overline{10H}$ at D 4302/14 $\overline{20H}$ at D 4302/13  $\overline{50H}$ at D 4302/10 	a1 ... g1 a2 ... g2 St0 X 4301  (3.4...4.3)V
Test A6	A6	$\overline{40H}$ at D 4302/11 	D0 ... D7 to X 4303/1...8 A0 ... A2 at X 4304/6,7,8 

1) of. Section 6.2.9. V24 interface/example 2

2) of. Sections 6.2.8. and 6.2.9.

6.2.7. Keyboard
Output signals.

Figure 12.

Taste	Hexa- code	847017								847027	FR
		1	2	3	4	5	6	7	8	9	
		PA6	PA5	PA4	PA3	PA2	PA1	PA0	IR	III	
EXT	00	U	U	U	U	0	0	0	1	1	} 3 ms
END	6d	1	1	U	1	1	0	1	1	1	
9	62	1	1	U	U	0	1	0	1	1	
4C	67	1	1	U	U	1	1	1	1	1	
DEL	76	1	1	1	U	1	1	0	1	1	
EXT FCT	20	0	1	0	0	0	0	0	0	0	
SCAN FCT	61	1	1	U	U	0	1	1	1	1	
SCAN	6C	1	1	U	1	1	0	0	1	1	
	64	1	1	U	U	1	0	0	1	1	
	66	1	1	U	U	1	1	0	1	1	
CALL 99	21	U	1	U	U	0	0	1	0	1	
CALL 90	22	U	1	U	U	0	1	0	1	1	
CALL	63	1	1	U	U	0	1	1	1	1	
END	73	1	1	1	U	0	1	1	1	1	
	65	1	1	U	U	1	0	1	1	1	
	30	U	1	1	U	0	0	0	1	1	
	31	U	1	1	U	0	0	1	1	1	
	32	U	1	1	U	0	1	0	1	1	
	33	U	1	1	U	0	1	1	1	1	
	34	U	1	1	U	1	0	0	1	1	
	35	U	1	1	U	1	0	1	1	1	
	36	U	1	1	U	1	1	0	1	1	
	37	U	1	1	U	1	1	1	1	1	
	38	U	1	1	U	0	0	0	1	1	
	39	U	1	1	U	0	0	1	1	1	
	2E	U	1	U	1	1	1	0	1	1	
	3b	U	1	1	1	0	1	1	1	1	
EXT EXT FCT	00	0	0	0	0	0	0	0	0	0	
	20	U	1	U	1	0	11	11	1	1	
	24	U	1	U	1	11	0	11	1	1	
keine Taste	70	1	1	1	1	0	0	0	1	1	

3 ms

0,5 ms

Für jede Taste kann der Code stattdessen erzeugt werden, wenn gleichzeitig die Taste EXT FCT gedrückt wird.

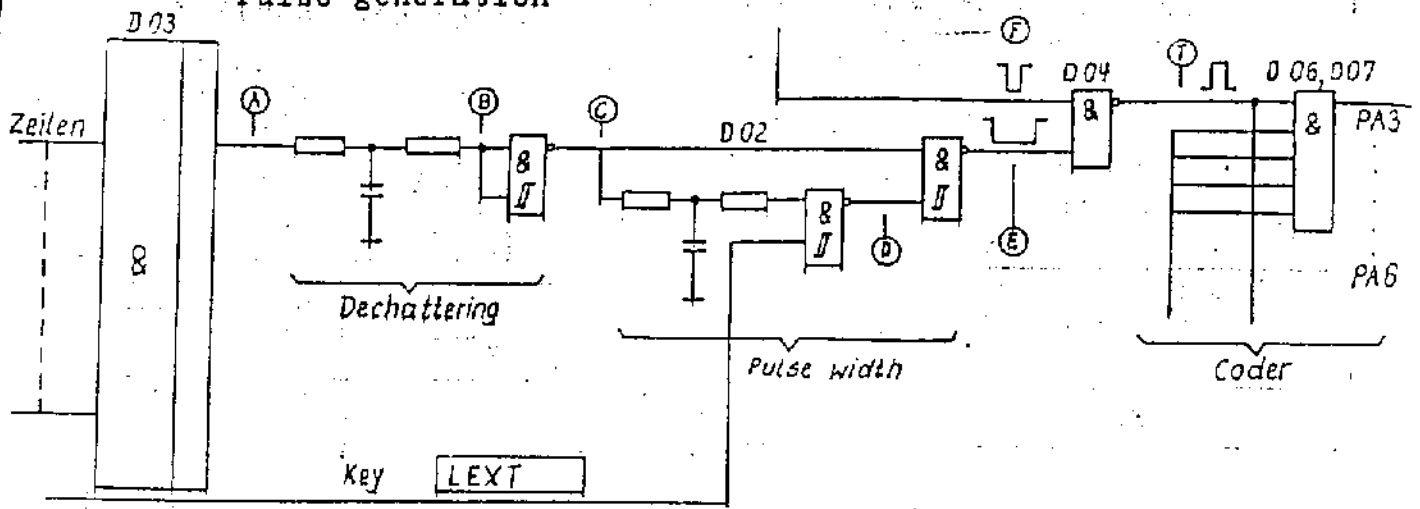
Code can be generated for each key if EXT FCT is pressed simultaneously

- Low/high levels

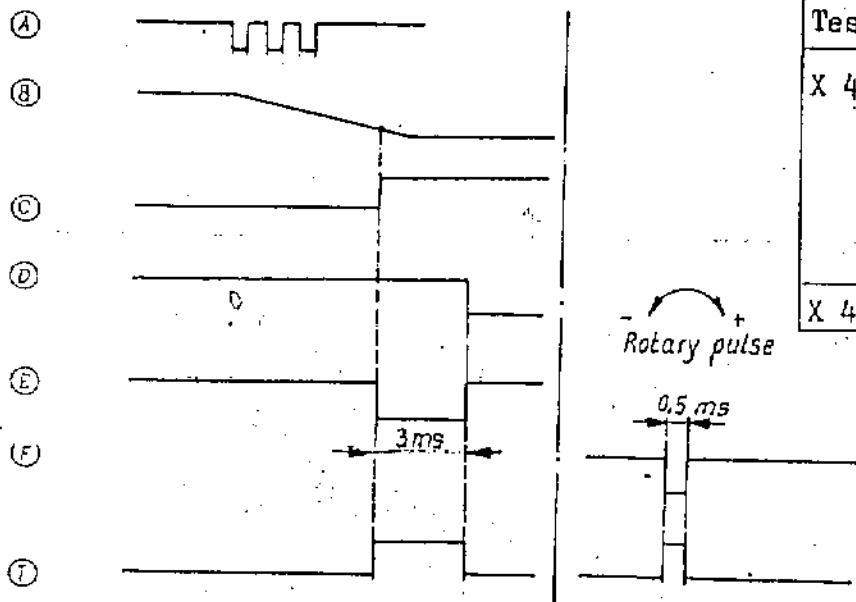
Static L/H levels are to be provided at the outputs by depressing the respective key. Checks should be performed according to the scheme below.

Outputs		Low		High	
		Key	Level	Key	Level
X 4701/8	\overline{TR}	"CALL 99"			
7	PA 0	"EXT" and "EXT FCT"	-0.5 V	"7"	>4.0 V
6	1				
5	2				
4	3				
3	4				
2	5				
1	6				
X 4702/6	\overline{TN}				

- Pulse generation



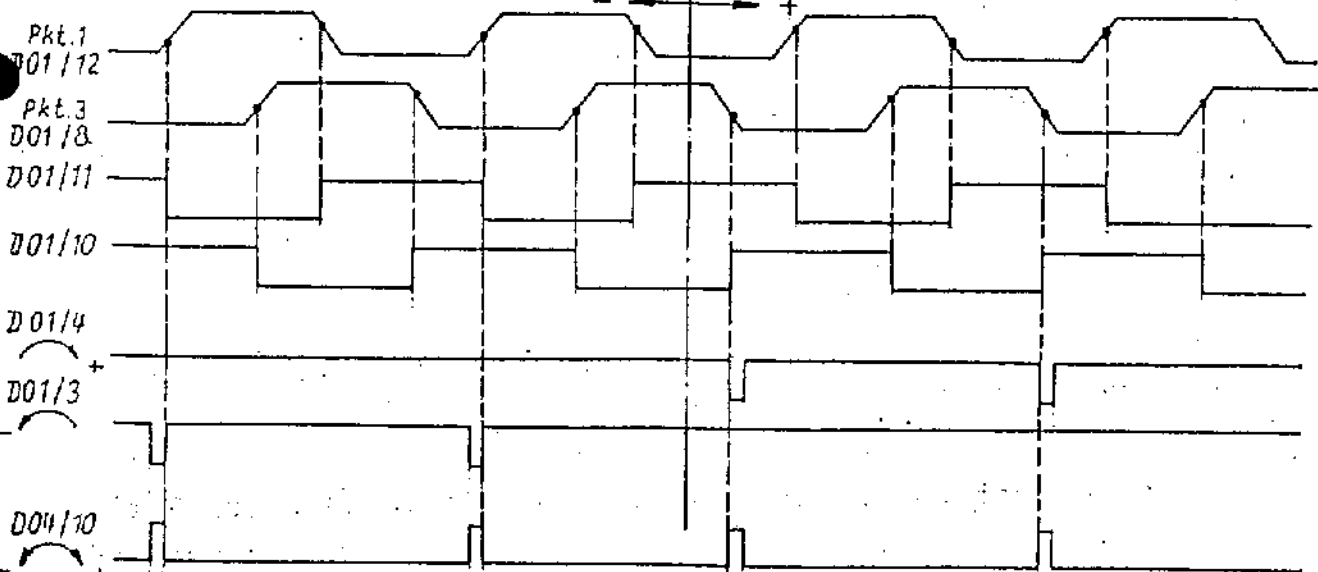
Key pulse



L/H level

Test point	L (V)	H (V)
X 4701/1 PA 6	< 0.5	> 4.5
7 PA 0	< 0.5	> 4.5
8 TR	< 0.5	> 3
X 4701/6 TN	< 2.6	> 3

- Pulse diagram for rotary pulse generator



6.2.8.

- Digital display

Voltage curve in test A1

Segment	Test point at X 4601	\hat{U}	
a1 ... g1	A4, B3, B13; B12 A13, A3, B4	~3.4 V	
a2 ... g2	A1, A2, A11, A12 B11, B2, B1		
p1, p2 St0...St4	A5, B10 A8, B9, B7, A10 B8	~4.3 V	
LED EXT	A9	~4.3 V ~4.7 V	

- LED row

Voltage values

Position S 4001	U at input	Point	U at point 15	Lighting LED
$\Delta F \times 1$	0 V	04	2.7 V ₌	V 17
$\Delta F \times 2$				V 17
E γ	4.8 V ₌	19		V 17
U _{AF}	1.4 V _~ (1 kHz)	03	4.7 V ₌ (1)	V 22

1) correction with R 4631

Check entire row with test A3 according to the Equipment documentation Section III/5,

S 4001 to E γ

0.2.3. Register and interface

- Register and interface matrix

The receiver setting is stored in the 12 register circuits D 4504 to D 4515 that form the register and interface being arranged as matrix (7 rows/8 columns). The rows are the addresses, the columns the data.

Assignment of the circuit function

A \ D	7	6	5	4	3	2	1	0
1	D 4505 100Hz				D 4504 10Hz			
2	D 4707 10 kHz				D 4506 1 kHz			
3	D 4509 1 MHz				D 4508 100 kHz			
4					D 4510 10 MHz			
5	D 4512 MOD				D 4511 B			
6	D 4514 SEL				D 4513 SEL			
7					D 4515 GC			

Example

Short-time reaction at $\Delta F \approx 1 \text{ kHz}$

Setting

73 B 12345.67

SEL 1

GC 4

A \ D	7	6	5	4	3	2	1	0
1	0	1	1	0	0	1	1	1
2	0	1	0	0	0	1	0	1
3	0	1	0	0	0	1	0	1
4	0	0	1	0	0	0	1	1
5	0	1	1	1	1	1	0	0
6	0	1	1	0			0	1
7						1	0	0

Note:

Data for B stored in inverted form. The letterings on the lines at the outputs of the register circuits correspond with this matrix.

48

Example: 3/5 means address 3/data bit 5, i.e. bit 2¹ of the 1-Hz digit of the frequency.

- The frequency data correspond with the decimal places in the 8-4-2-1 code. Output is performed via drivers D 4516 to D 4520. The output lines are marked in accordance with the decimal points. The levels are CMOS levels.

Example: Setting to 1.23 kHz

Frequency	x 1 kHz				x 100 Hz				x 10 Hz			
	d3	c3	b3	a3	d2	c2	b2	a2	d1	c1	b1	a1
Logic condition	0	0	0	1	0	0	1	0	0	0	1	1
X 4501	B20	B19	B18	B17	B24	B23	B22	B21	B28	B27	B26	B25

- The selector data are derived automatically from the frequency i.e. the interconnection is contained in the ROM test. The output lines go directly out from the store circuits; the voltages are CMOS levels. For MOD, B and GC the store data are decoded and logically connected. The output signals are generated via driver stages.

- Check of the register and interface outputs

Precondition: Input and display in order. Input signals A0...A2 at X 4503 and D0...D6 at X 4504 available, if not, check 40 H at input-output logic (cf. Section 6.2.6.).

Correct display does not indicate proper output of the register and interface.

Checking the outputs is performed with test A6

Setting

A6

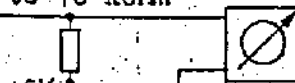
(test 6)

With key switch digits 00 to 99 further ones after the other; Check with this the logic conditions at the soldering side according to the table for register and interface test. (cf. Fig. 13) Observe the following:

X 4501/a 16 This point lies next to +18 V
Be cautious with test prod.

X 4505/B7 }
/B9 } Check of the logic conditions with pull-up
resistance 3.3 kohm to 10 kohm

X4505
B7, B9



X 4501/A 16 }
X 4505/B5 }
/B9 }

At these points, carry out an additional check of the short-time reaction at $\Delta F \approx 1$ kHz.

Table Display in testing procedure

	Measur. point	Register and interface test										Level 0/1	
		00	11	22	33	44	55	66	77	88	99		
F	X4501/B3	0	0	1	1	0	0	1	1	0	0	$\approx 0,8V / \approx 2,4V$	
	B4	0	1	0	1	0	1	0	1	0	1		
	Code 8421 corresponds to d o b a												
	x 10 Hz	B25	0	1	0	1	0	1	0	1	0		1
	B26	0	0	1	1	0	0	1	1	0	0		
	B27	0	0	0	0	1	1	1	1	0	0		
	B28	0	0	0	0	0	0	0	0	1	1		
SEL	X4501/A26	0	1	0	1	0	1	0	1	0	1	$\approx 0,5V / \approx 4,5V$	
	A27	0	0	1	1	0	0	1	1	0	0		
	A28	0	1	0	1	0	1	0	1	0	1		
	A29	0	0	1	1	0	0	1	1	0	0		
	B29	0	0	0	0	1	1	1	1	0	0		
MOD	X4501/A25	0	1	0	0	0	0	0	0	0	0	$\approx 0,2V / \approx 17,5V$	
	A24	0	0	1	0	0	0	0	0	0	0		
	A23	0	0	0	1	0	1	0	0	0	0		
	A22	0	0	0	1	0	1	0	0	0	0		
	A21	0	0	0	0	1	0	1	0	0	0		
	A20	0	0	0	0	0	1	1	0	0	0		
	A19	0	0	0	0	0	0	0	1	1	0		
	A18	0	0	0	0	0	0	0	0	0	1		
	A17	0	0	0	0	0	0	0	1	1	1		
A16	0	0	0	0	0	0	0	0	1	1			
B	X4505/B1	0	1	0	1	0	1	0	1	0	1	$\approx 1V / \approx 6V$	
	B2	0	0	1	1	0	0	1	1	0	0		
	B3	0	0	0	0	1	1	1	1	0	0		
	B4	0	0	0	0	0	0	0	0	0	1		
	B5	0	0	0	0	0	0	0	0	0	1		
GC	X4505/B7	0	1	0	1	0	1	1	1	1	1	$\approx 0,2V / \approx 3V$	
	B8	1	0	0	1	1	1	1	1	1	0		
	B9	1	1	1	1	1	0	1	1	1	0		

Figure 13

- Short-time reactions

In case of frequency changes of ≈ 1 kHz the control computer supplies the output GC = 8 that initiates through the monostable flipflop (D 4523) a dynamic behaviour of lines FS 1/0, \downarrow and U_{block} . A short lighting up of V 4623 (right LED) presents in the LED row.

Setting 73 E 0.00

$dF \approx 1$ kHz

Test point	Line	Pulse	Condition
X 4501/A 16	FS 1/0		MOD 8 or 9
X 4505/B9	\downarrow		GC \neq 5
X 4505/B5	U_{block}		

$T = 125 \dots 155$ ms

- Receive blocking (cf. Equipment documentation, Section II/2.7.)

The blocking signal of $+ (3 \dots 15)$ V at X 0013/X 0014 and bandwidth B = 9 have the same effects:

Test point	Line	Logic condition	Level
X 4505/B4	5/3	1	≈ 1 V / ≈ 6 V
X 4505/B5	U_{block}	1	≈ 1 V / ≈ 6 V
X 4501/A16	FS 1/0	0	≈ 0.2 V / ≈ 12 V

- SCAN STOP

The control signal at X 0015/X 0016 acts via N 4501/8 and D 4501/4 on PB \emptyset .

Function	U_{\dots} at X 0015/X 0016	PB \emptyset at X 4502/6	Level 0/1
SCAN	-15 V ... +0.8 V 1)	1	≈ 4.5 V
SCAN STOP	+3 V .. +15 V	0	≈ 0.5 V

1) Control signal -15 V ... +8 V is equivalent to 'sockets open'.

5/1

Precondition: Function of the signal path in order.

Setting 1 16 E 0.00 GC 1

Set f_{AF} to 1 kHz with A1 \approx

Set U_{AF} to 0 dB_m (0.77 V) at X 1020/A - B with \approx

Frequency F = 1.50 kHz

Check if $U_{AF} \approx -12$ dBm

Setting 2 48 E 1.00 GC 1

U_{AF} to 0 dBm as above

Frequency F = 2.50 kHz

Check if $U_{AF} \approx -3$ dBm

If U_{AF} is not adjustable or in case of distortions, check level with setting 1:

Incoming AF voltage at X 4505/A 13 ~ 0 dBm (0.77 V)

outgoing AF voltage at X 4505/B 13 ~ -12 dBm (0.2 V)

Checking and balancing the control voltage linearization

Precondition: Function of the signal path in order.

Do not unscrew front panel of the plug-in; balancing elements are accessible from above (cf. Figure 9). Balancing requires feeding of a defined aerial signal with calibration level. Use aerial socket X 0001 at the casing rear; $Z = 75$ ohm. The voltages to be supplied are emf ratings.

Setting 47 E 4500.00 GC 1, SEL 0

Frequency setting on test oscillator 4501.00 kHz

Make use of A3, perform balancing according to the table below:

Aerial emf	Number	Balancing element	Remarks
30 dB (μ V) \approx 32 μ V	15	R 45 145	} alternating until residual error = 0
90 dB (μ V) \approx 32 mV	45	R 45 146	
10 dB (μ V) \approx 3.2 μ V	05	R 45 148	
120 dB (μ V) \approx 1 V	60	R 45 147	

Check by repetition

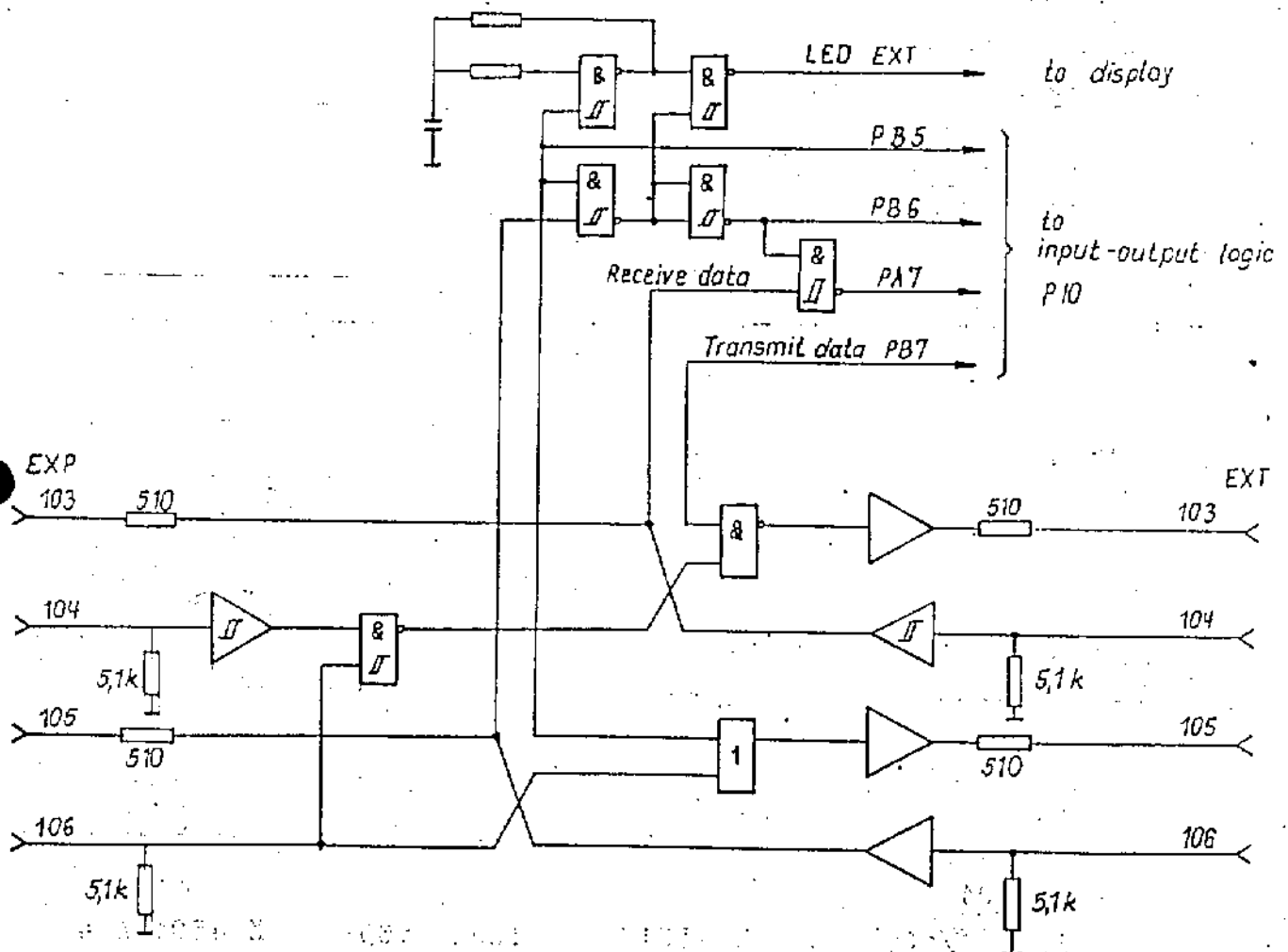
In balanced condition, the display fault amounts in digits to ± 2 , i.e. to ± 4 dB (μ V).

- V-24 interface

Lines

- 101 Protective earth
- 102 System earth
- 103 Transmitting data to data transmission equipment (DUE)
- 104 Receiving data from DUE
- 105 Request to transmit to DUE
- 106 Ready for transmission from DUE

. Schematic circuit diagram



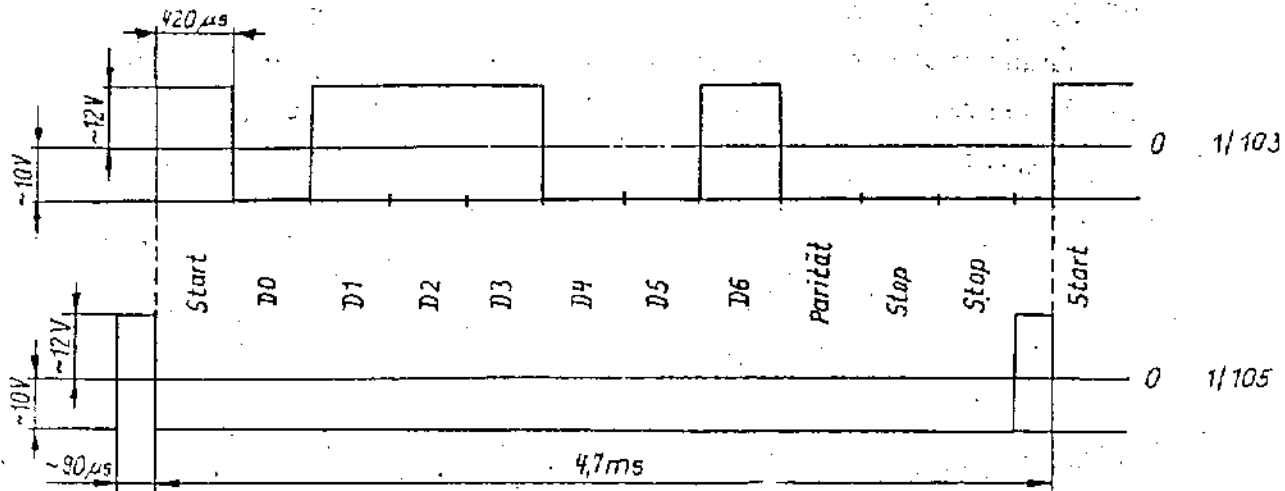
Setting test A2

Double-beam oscillograph

B channel at line 1/103, X 0005/E - A, B (⊥) } A channel
 A channel at line 1/105, X 0005/C - A, B (⊥) } synchronizes
 B channel

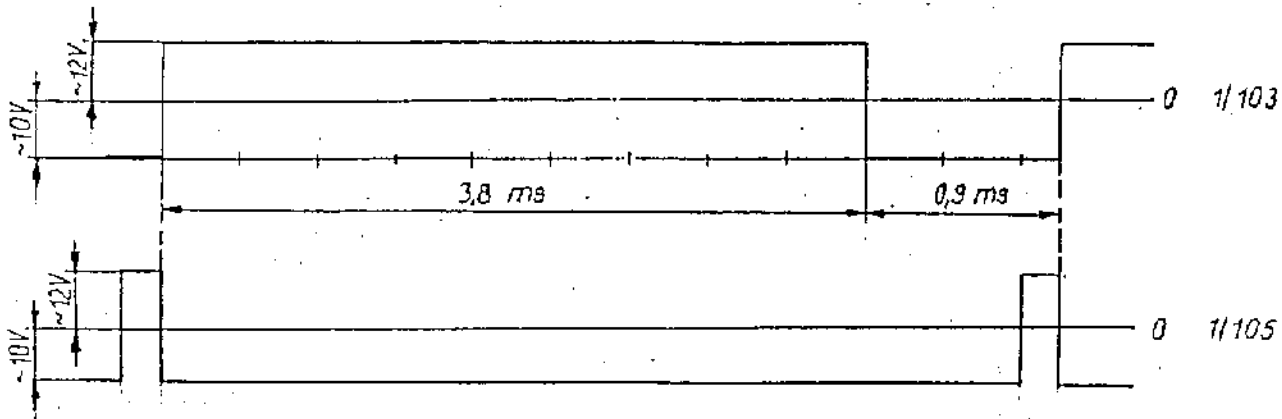
Oscillograph pulse curve

Example 1 Key 1 , 31 H



If no double-beam oscillograph available, select key EXT , 00 H. Oscillograph lines 1/103 and 1/105 separately.

Example 2 Key EXT , 00 H



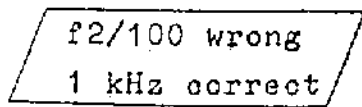
If no pulses can be detected, trace the signal back up to X 4501

Line 1/103 X 4501/A2, line 1/105 X 4501/A 4

6.3. Frequency processing

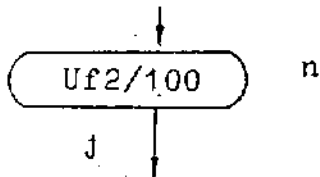
6.3.1. Troubleshooting sequence

The test programs for troubleshooting are given in the following in accordance with the principle of frequency processing. Each program starts with indication of the fault, e.g.



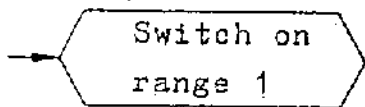
that means that frequency f2/100 is wrong, the 1-kHz signal correct.

After that, different test measurements are carried out which are indicated as abridged questions, e.g.



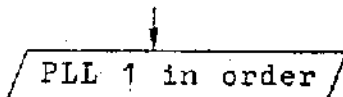
that means that the voltage or the voltage curve Uf2/ are available as represented in the General diagram.

The measurements indicate which component is to be checked. The required test program or test instructions are given, e.g. → PLL2



For each test program the measuring points are given in the opposite diagrams.

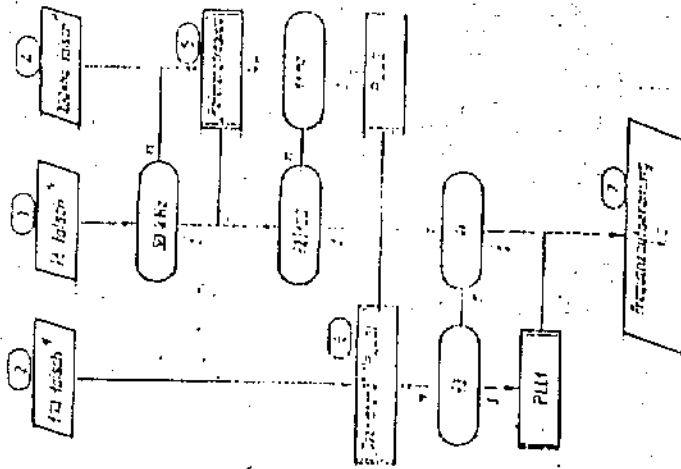
The test program is terminated with the information that the component to be tested is troublefree, e.g.



Wird gefertigt
Kolligang
Wird gefertigt

6.3.2. Frequency processing - outline.

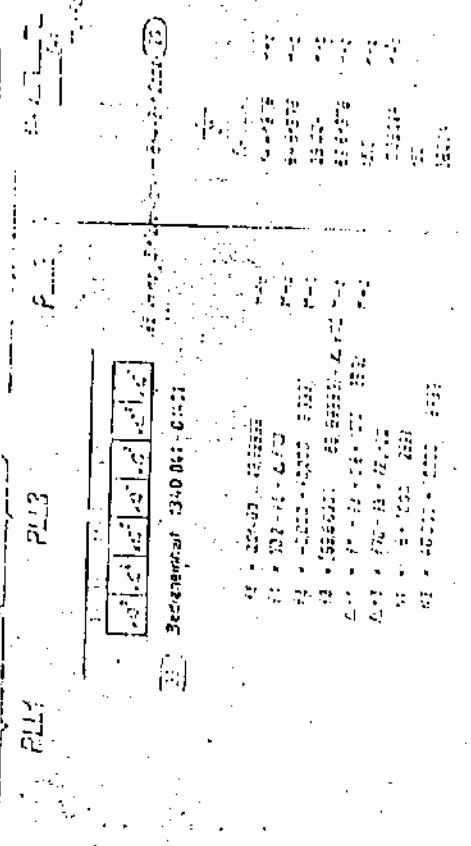
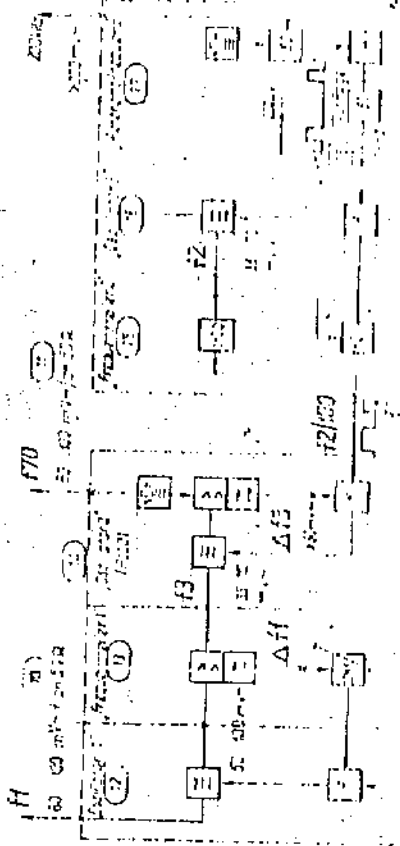
1 Programm für die Fehlersuche



F1: Busch
 F2: Filter
 F3: 50 kHz
 F4: 100 kHz
 F5: PLL
 F7: Frequenzmessung

2 Vereinfachter Übersichtsschaltplan - Frequenzen und Pegel

Frequenzverarbeitung 1
 Frequenzverarbeitung 2



Frequenzverarbeitung - Übersicht

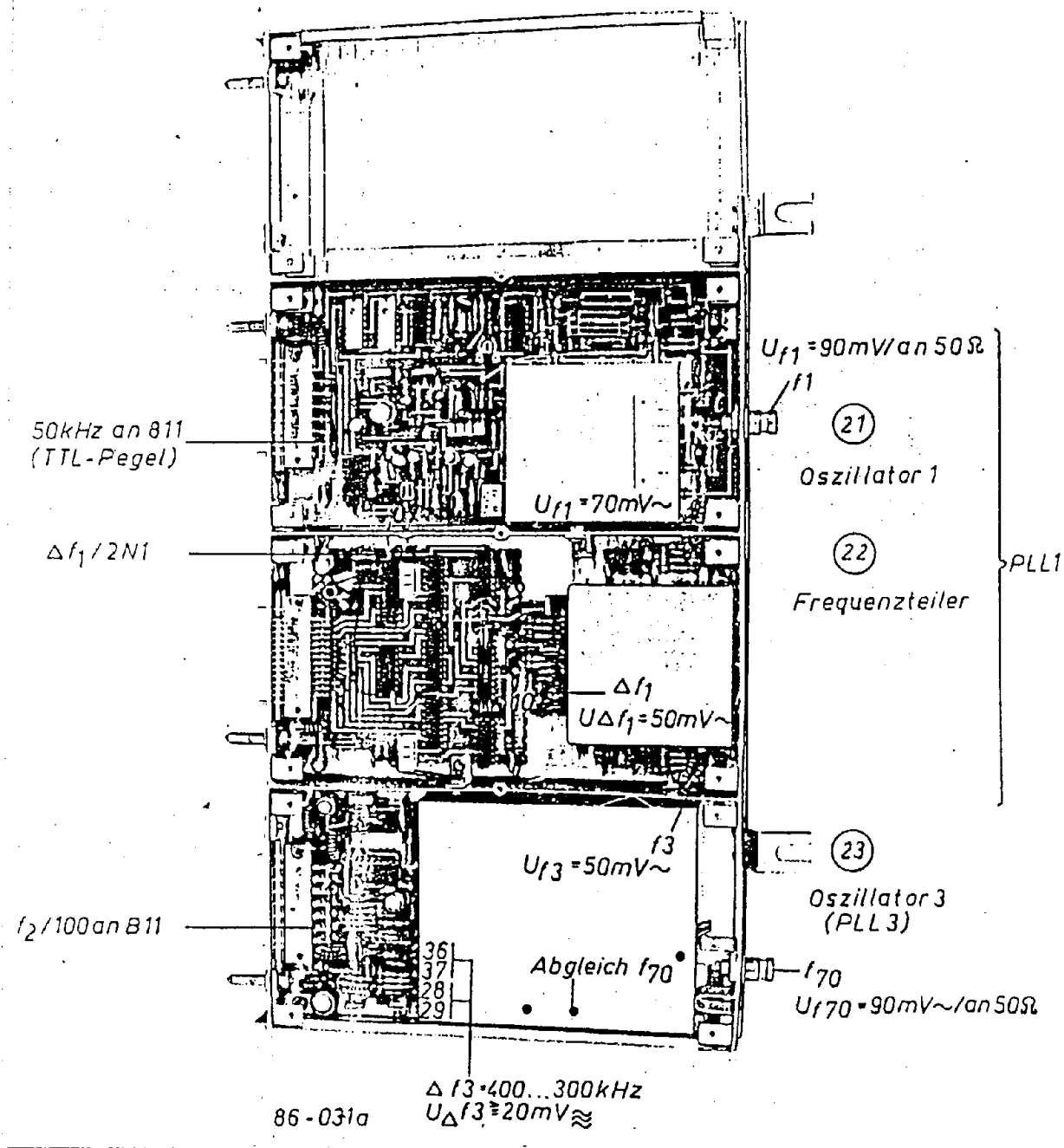


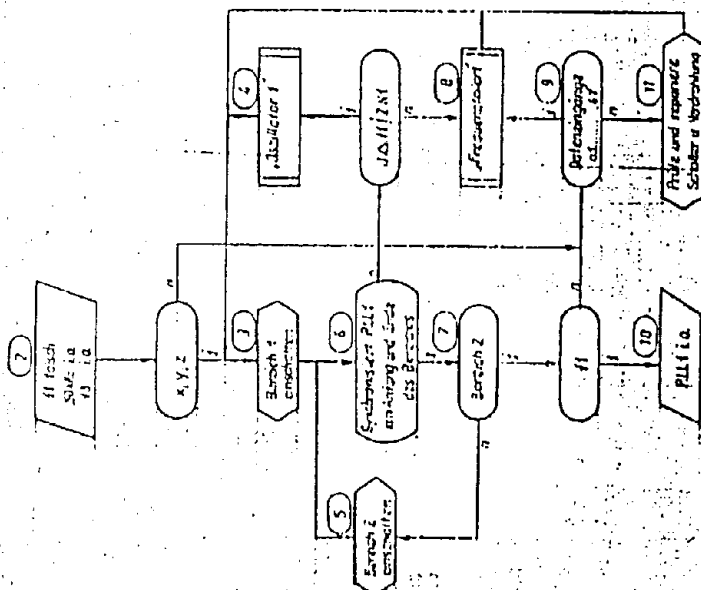
Figure 14
 Frequency processing 1 1340.041-01211

Dieser Zigaretten-
 filter
 wird verfoigt

57

6.3.3. Phase-lock loop 1 (PLL1)

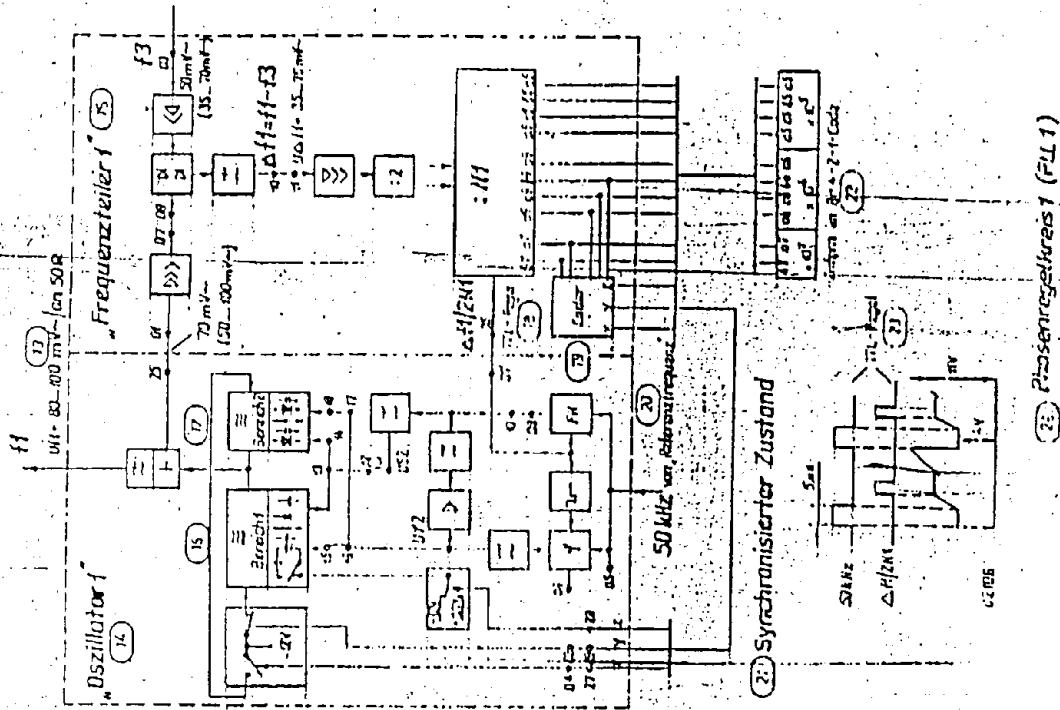
7 Prüfprogramm PLL1



f1	700	700	700
f2	650000	650000	650000
f3	100	100	100
Δf	100	100	100
M	5	10	20

Bereich	f1 in kHz	x y z
10	00	1 0 1
16	20	1 0 0
2	100	0 1 0

12 Blockschaltbild PLL1



130

(1) synchronisierter Zustand

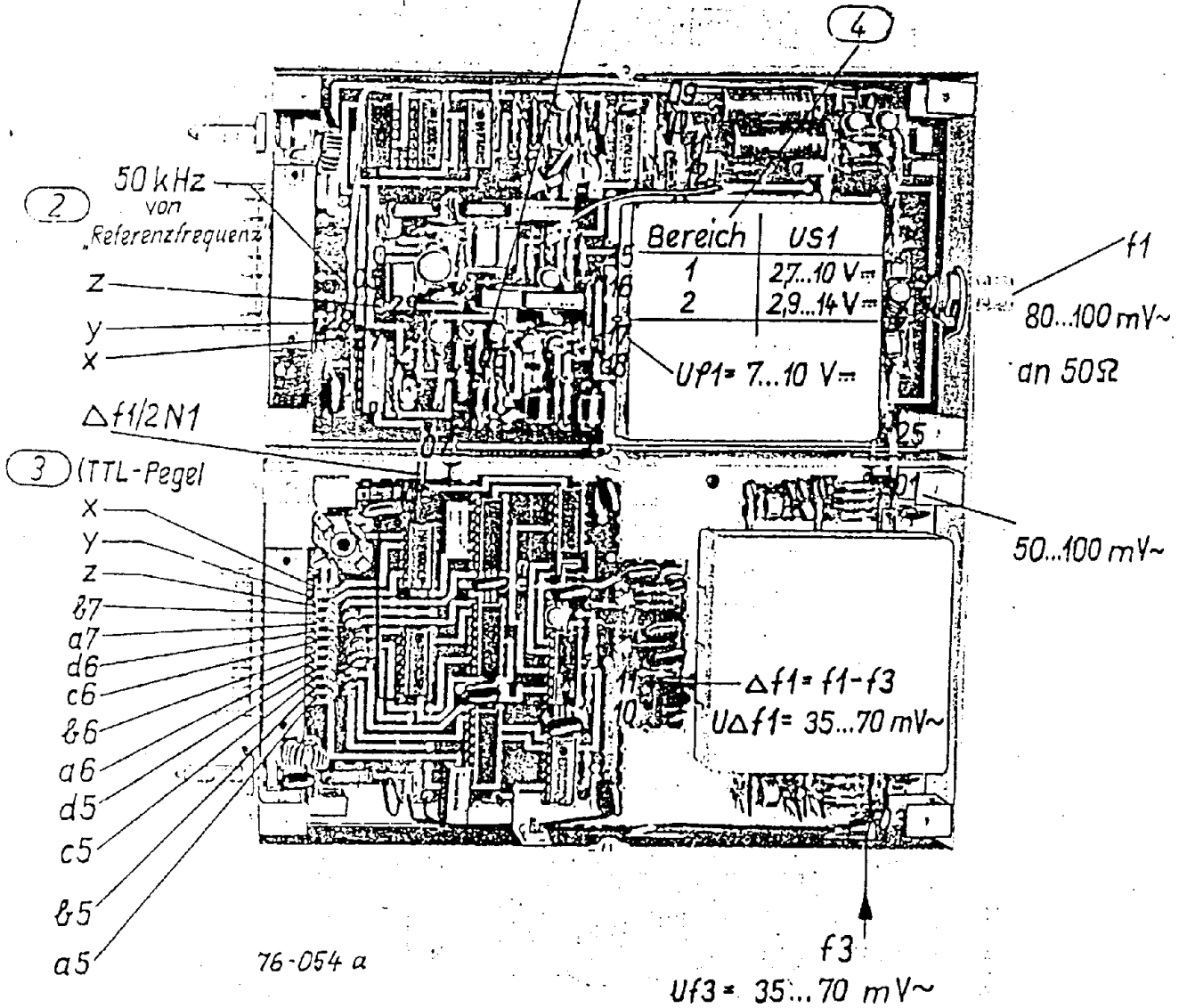
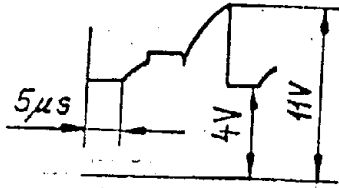
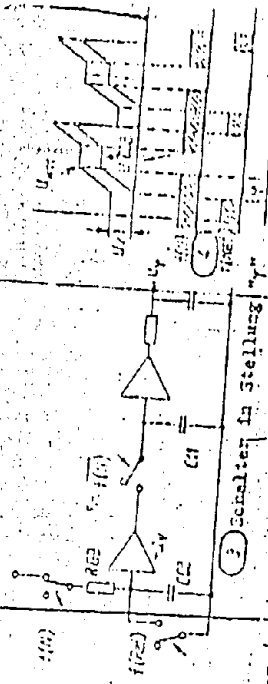


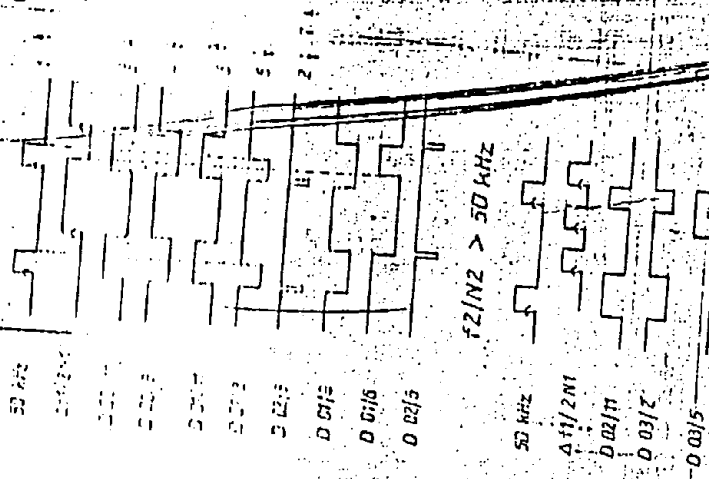
Figure 15
Positions of test points PLL1

6.3.4. Oscillator 1

2) Arbeitsweise des Frequenzdiskriminators



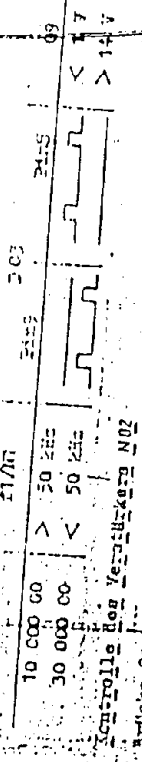
3) Impulschema des Frequenzdiskriminators



Oszillator 1

7) Kontrolle des Frequenzdiskriminators (Frequenzhilfe)

3 C1, 302, 303, V10, V11, u. V12
 Brücke 09...10 prüfen
 Brücke 11...12 prüfen
 an 12 ca. +3 V anlegen (C15 hat Zwickspannung)



Kontrolle des Verstärkers N02
 Brücke 09...10 prüfen
 Brücke 11...12 prüfen
 mit 2225 erarbeiten

Abgleich der Oszillatordfrequenz
 Form 2225, V2125, V2125 oder V2125 verwendet werden. Ist die
 Abgleich der Oszillatordfrequenz notwendig, der Abgleich erfolgt im Bereich 1
 mit C24 und im Bereich 2 mit C34 durch Wechseln der Kondensatoren.
 Abgleichbedingungen (mit Abgleich-Kappe gemessen):

Frequenz-Einstellung	U _s an Zkt. 11/2/8, 2/3
1. 10 000 G0	2,7...2,9 V - U (1.)
2. 30 000 G0	< 14 V
3. 31 000 G0	Synchronisiert?
4. 00 000 G0	U (1.) - 0,2 V
5. 09 999 99	9...11 V

Abgleich des Frequenzdiskriminators
 Einstellen mit R2125
 U_p 7...10 V an Zkt. 15...18 bei f_e 20 000 G0
 Oszillogramm an C2108 und R2117 besichtigen!

Test sequence

No output voltage f1

1. UC45 or UC47
2. U 1 (15...18)
3. J81 (12)
4. Does oscillator work?

Control circuit does not synchronize (06)

1. Operating voltages
2. 50 kHz (ref) (05)
3. $\Delta F1/2N1$ (07)
4. U f 4 (15...18)
5. U81 (12)
6. Open bridge 11...12, apply approx. +8 V dc to 12, synchronize with frequency switch '10 MHz' and '1 MHz'
7. Check capture aid and N 02
8. Balance phase discriminator

6.3.4. Oszillator 1

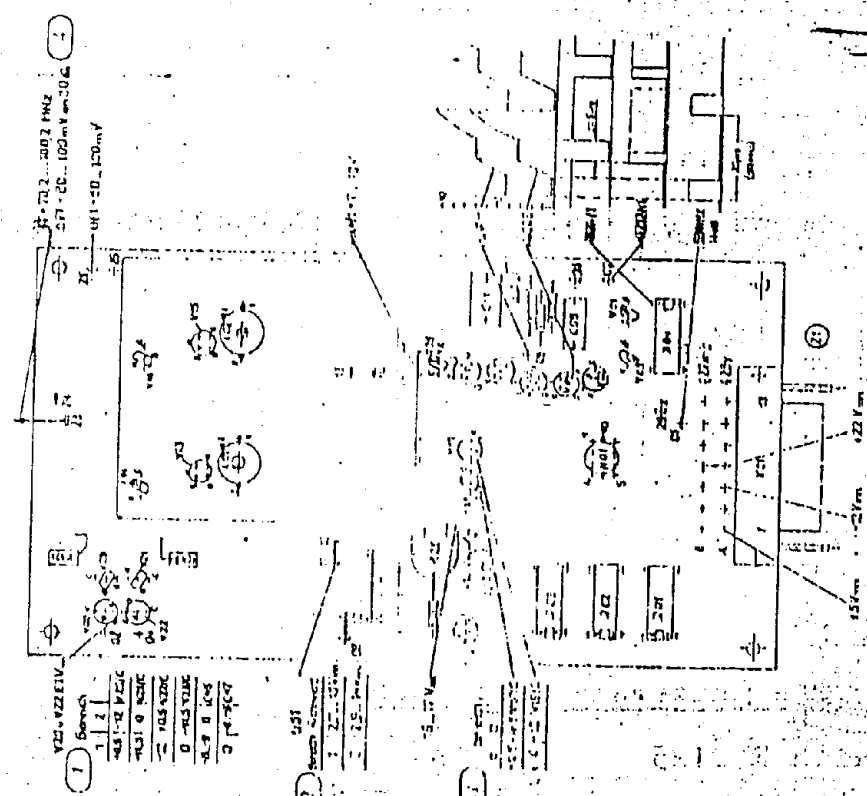
5
Zusatz

Keine Ausgangsspannung 71

1. UC45 bzw. UC47
2. J 1 (45..18)
3. US1 (42)
4. schwach Oszillator 7

1. Elektronen-Verschleif-Licht (66)
2. Betriebsbedingungen
3. 50 kHz (67)
4. AP1/200 (67)
5. 100 (65..18)
6. 100

Es wird ...
 die ...
 ...



Check of the frequency discriminator (capture aid)

D01, D02, D03, V10, V11 and V12

Open bridge 09 ... 10

Open bridge 11 ... 12

Apply approx. +8 V dc to 12 (suitable voltage applied to C1E)

f _e	f ₁ /N1	D03		09
		Pin 9	Pin 5	
10 000 00	> 50 kHz			< 1 V
30 000 00	< 50 kHz			> 14 V

Check of the amplifier N 02

Open bridge 09 ... 10

Open bridge 11 ... 12

Adjust with R 2125

$U_{\text{pin 4}} \gg U_{\text{pin 5}} \longrightarrow U(11) < 2 \text{ V}$

$U_{\text{pin 4}} \gg U_{\text{pin 5}} \longrightarrow U(11) > 13 \text{ V}$

Balancing the oscillator frequency

After replacing V 2125, V 2126, V 2128 or V 2129 the oscillators have to be balanced. Balancing is performed in range 1 with C24 and in range 2 with C34 by exchanging the capacitors.

Balancing conditions (had measurement been performed with screening cap?)

Frequency setting	U_S at point 11 P 8, R_1 3 Mohm
1. 10 000 00	2.7 ... 2.9 V = U (1.)
2. 30 000 00	< 14 V
3. 31 000 00	synchronized ?
4. 00 000 00	$U(1.) - 0.2 \text{ V}$
5. 09 999 99	9 ... 11 V

Balancing the phase discriminator

Setting with R 2125

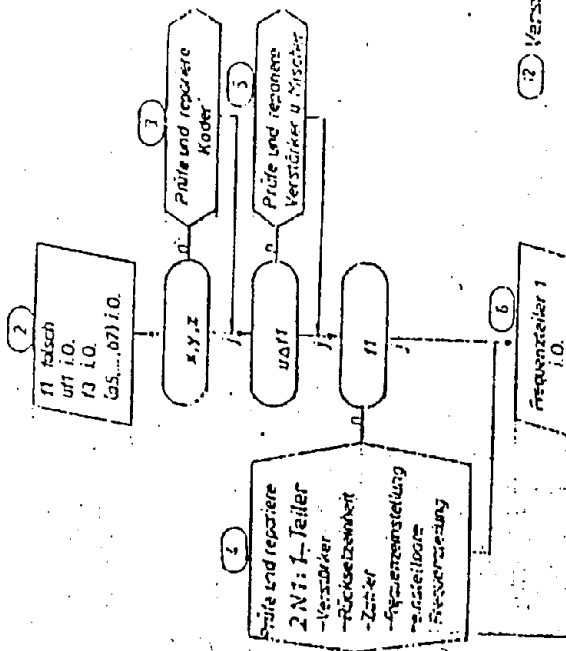
$U_{\varphi} = 7 \dots 10 \text{ V}$ at point 15 ... 18 at $f_E = 20 000 00$

Observe oscillogram at C 2108 and R 2111

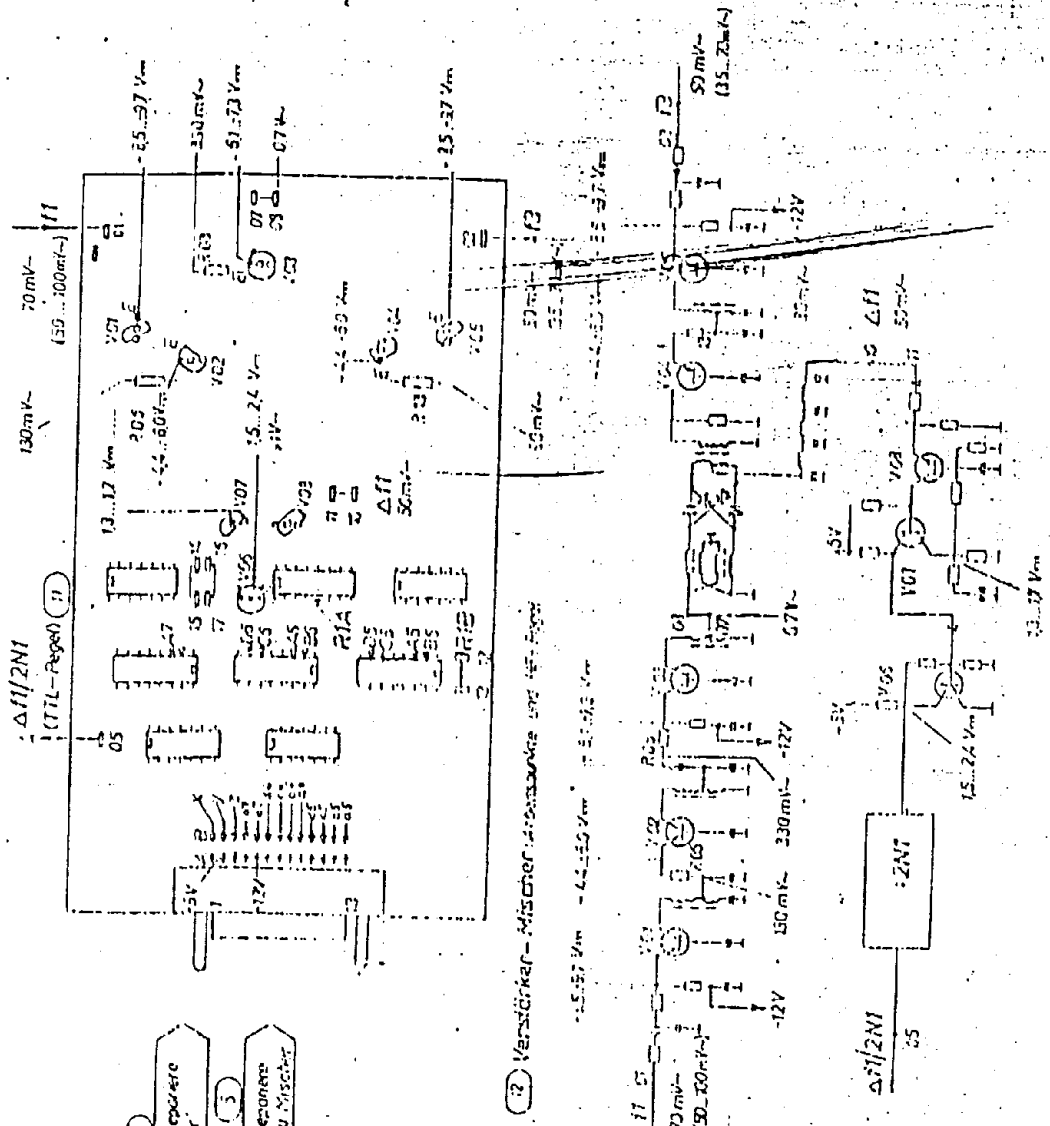
Weiterempfehlung
 Freigabe: 1988
 e wird verbleibt

6.3.5. Frequency divider 1

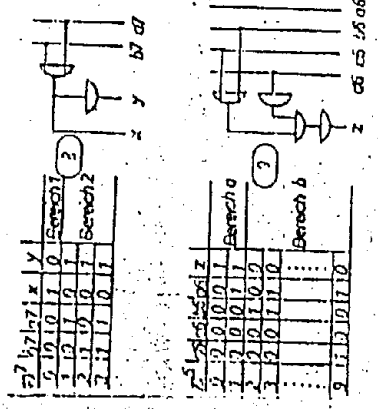
1 Prüfprogramm Frequenzteiler 1



10 Lage der Meßpunkte

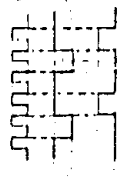


3 Kodes für Oszillator 1-Bereiche



7 Prüfung des Einstellbaren Frequenzteilers 1

-Rücksetzeinheit (3:1-Teilung)



Teil an 0/15
R1A an 0/5
R1B an 2

- Buchen 2 - 3 offen
- Buchen 4 - 5 verbunden
- Buchen 6 - 7 offen
- Buchen 8 - 9 verbunden

• U_{eff} = 50 mV_{eff}

-Zähler

U_{eff} = 200
• Buchen 2 - 3 offen
• Buchen 4 - 5 offen
• Buchen 6 - 7 offen
• Buchen 8 - 9 verbunden

-Frequenzinstellung

• Buchen 2 - 3 offen
• Buchen 4 - 5 offen
• Buchen 6 - 7 verbunden
• Buchen 8 - 9 verbunden

• U_{eff} = 50 mV_{eff}

-Einstellbare Frequenzteilung

• Buchen 2 - 13 verbunden
• Buchen 14 - 15 verbunden
• Buchen 16 - 17 verbunden

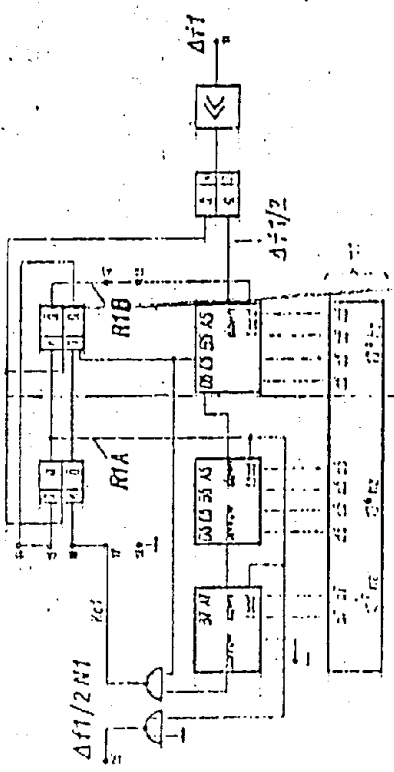
• U_{eff} = 50 mV_{eff}

3 für die Festsetzung kann man am Eingang (Punkt 11) ein Signal mit einem Pegel von 50 mV_{eff} aus einem externen Generator (P4) einspeisen

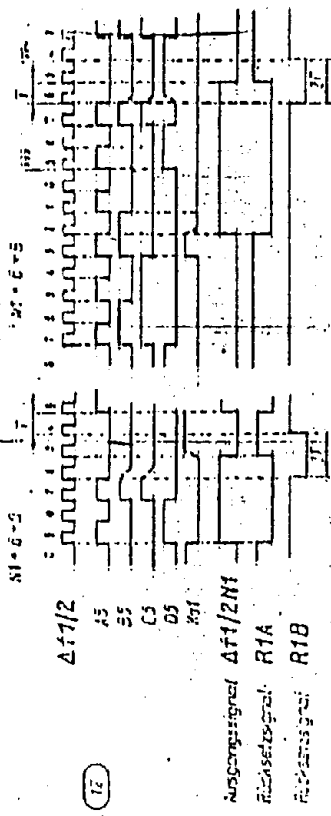
Einstellbarer Frequenzteiler 1

Eingangsfrequenz $\Delta f_1 = 0,5 + 2 \dots 255 \text{ kHz}$
Ausgangsfrequenz $\Delta f_2 / \Delta f_1 = 50$ kHz im höchsten Zustand von 201.
Teilerfaktor $2N1 = 2 \cdot (6 + N1)$
Zählentlang $N1 = 00 \dots 259$ Zifferwahl von 0 - 4 - 2 - 1 - Code
Zählende $n1 = 98$
Zählung nächstes, am 0 - 4 - 2 - 1 - Code

11 Blockschaltbild



Impulsdiagramme für 200 kHz



12 Frequenzteiler 1

Level balancing! Accomplish the following adjustments:

- With L 04 70-MHz voltage at 17 to minimum
- With L 02 70-MHz voltage at 17 to maximum
- With R 37 70-MHz voltage at 26
- With R 28 70-MHz voltage at 17

Frequency balancing

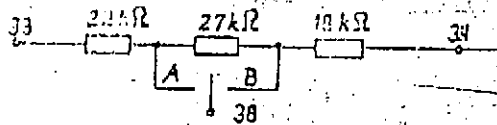
Balance $f = 70$ MHz with L 03, $\Delta f < \pm 150$ Hz.

6.3.6.2. f_3 oscillator

Level balancing f_3 :

Set 03 to ~ 50 mV/50 ohm with R 02 (tapping on the coil decoupling loop of L 01).

Frequency balancing f_3 :



Open bridge 38/39.

Apply positive voltage via opposite voltage divider to 38.

In position A (10 V dc) $f_3 > 69.7$ MHz; in position B (4 V dc)

$f_3 = 69.6$ MHz. If this cannot be reached, change C 04. Increasing C 04 causes decrease of frequency.

6.3.6.3. Phase discriminator

Image wave test:

$f_3 = 70$ MHz -- point 9/D02 = $U_{39} < 2$ V dc

Capture test:

$f_2/100 = 350$ kHz at 35

$f_3 = 69.650$ MHz -- wide negative pulses at point 5/D 02

-- $U_{39} = 13$ V dc

$f_3 > 69.650$ MHz -- wide negative pulses at point 9/D 02

-- $U_{39} = 4$ V dc

(The narrow negative pulses presenting at point 9/D 02 or 5/D 02 - approx. 50 ns - are only visible with appropriate setting of the oscillograph.)

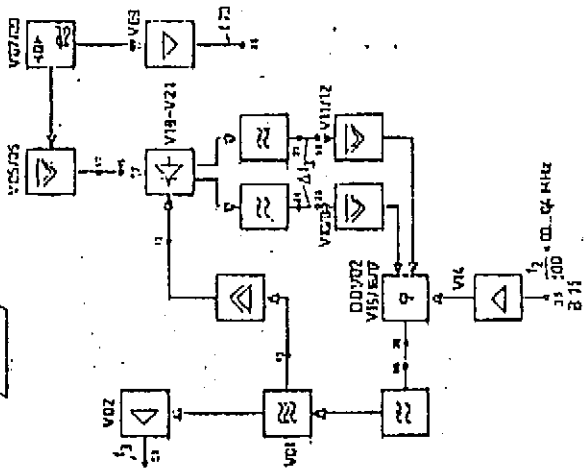
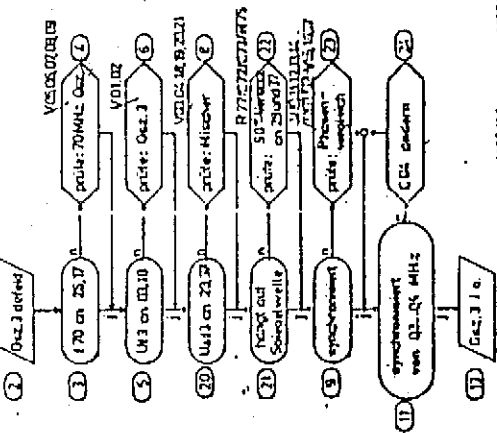
Phase discriminator:

Close bridge 38/39.

PLL synchronized ($U_{39} = 4 \dots 11$ V).

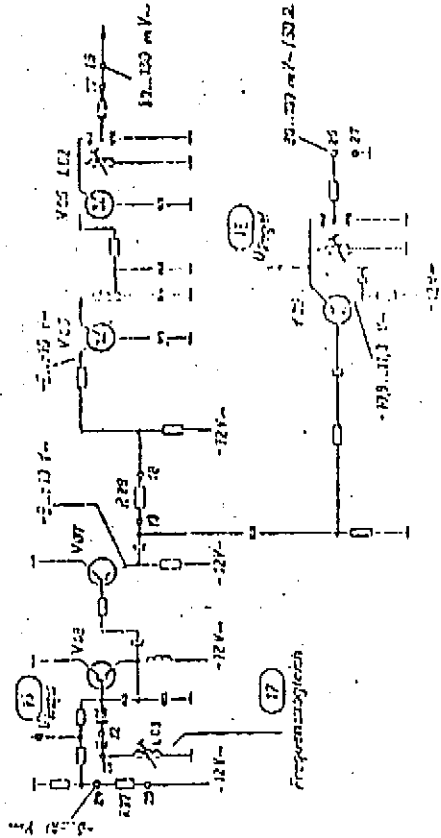
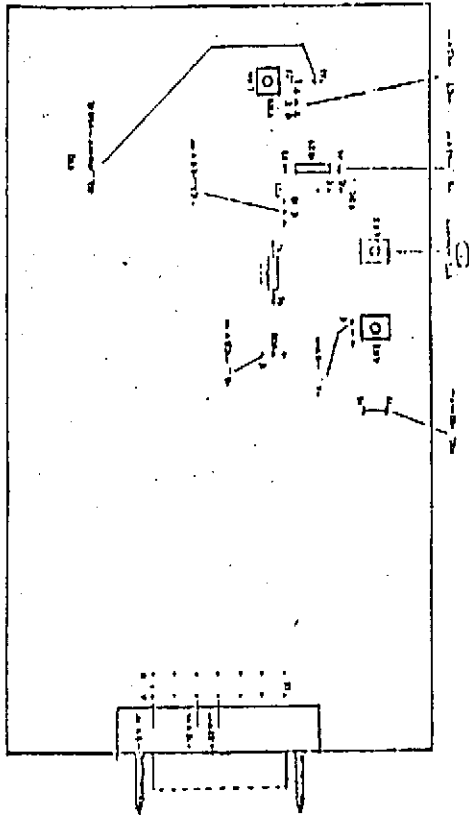
In case of triggering with $f_2/100$ the oscillograph supplies a stationary pattern of P30 and P54.

Prüfprogramm (oszillator 3) 1

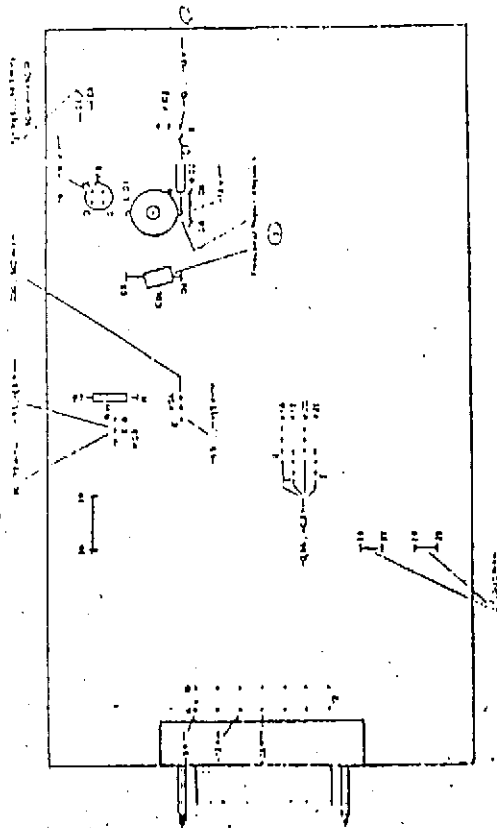


oszillator 3

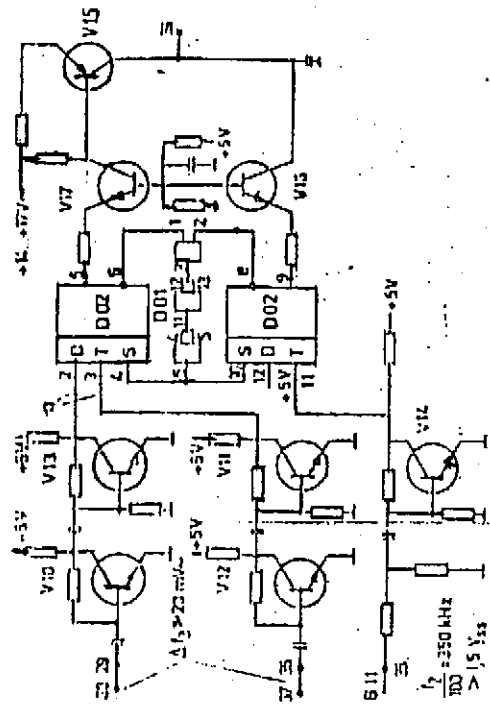
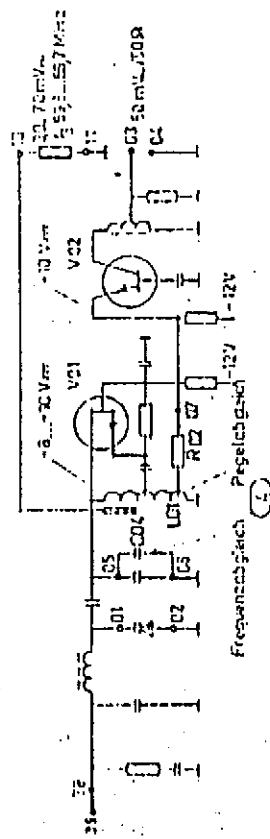
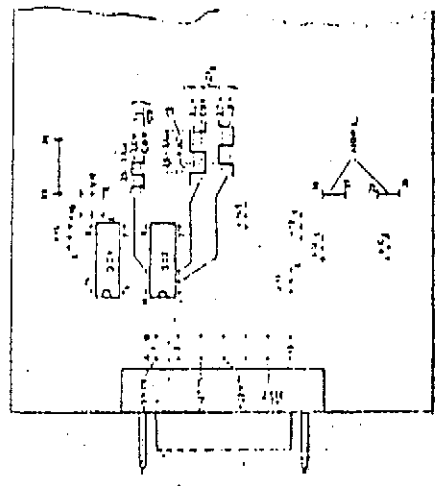
70 kHz - Oszillator



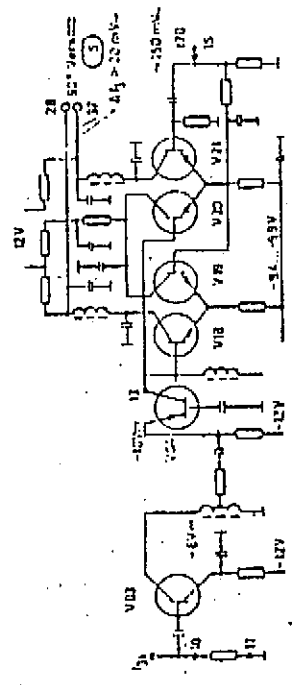
1) H-Oszillator und Verstärker



2) Phasenschieber



Oszillator 3



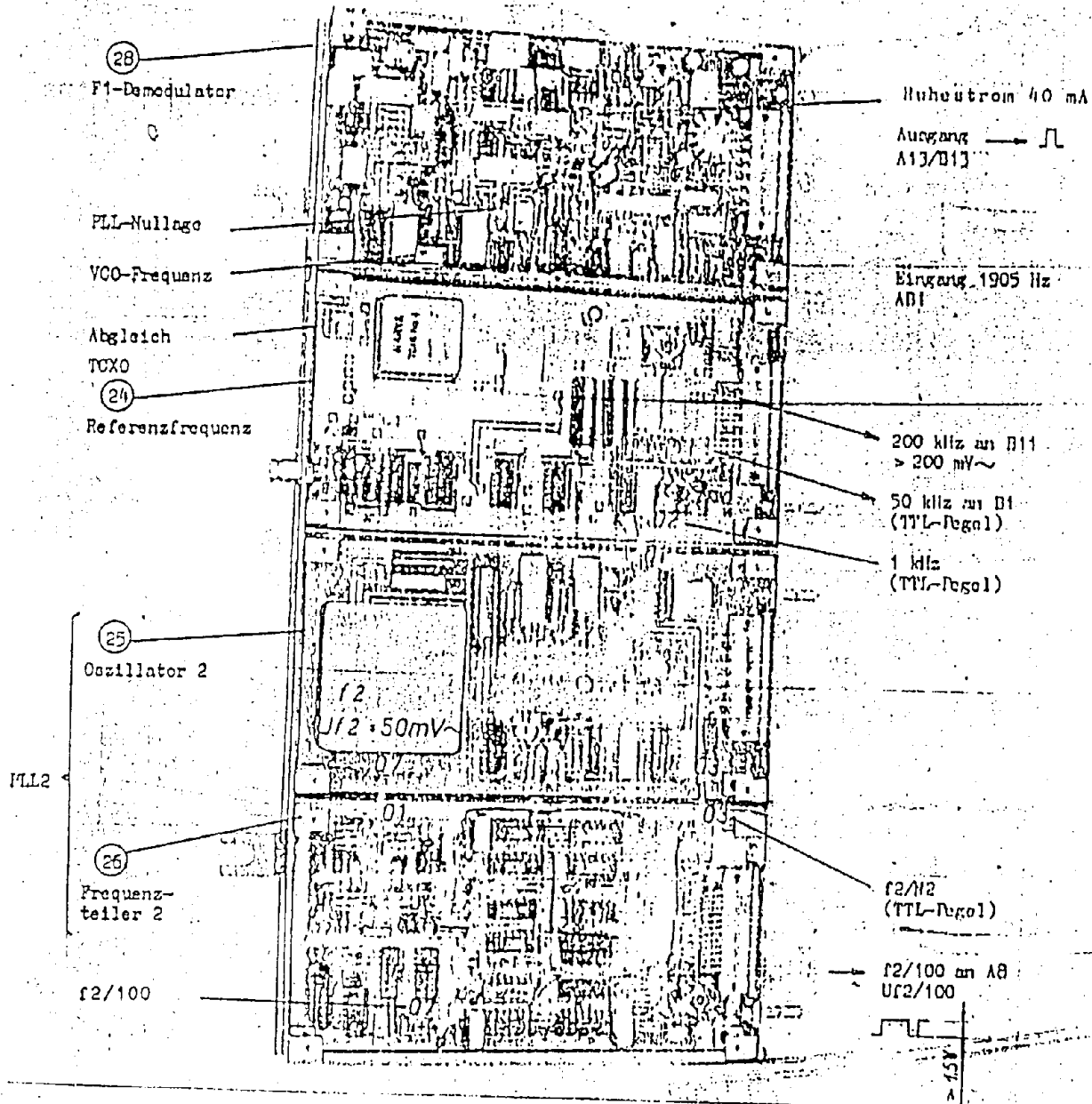


Figure 16 Frequency processing 2 and F1 - Demodulator 1340.041-01221

6.3.7. Phase-lock loop 2 (PLL 2)

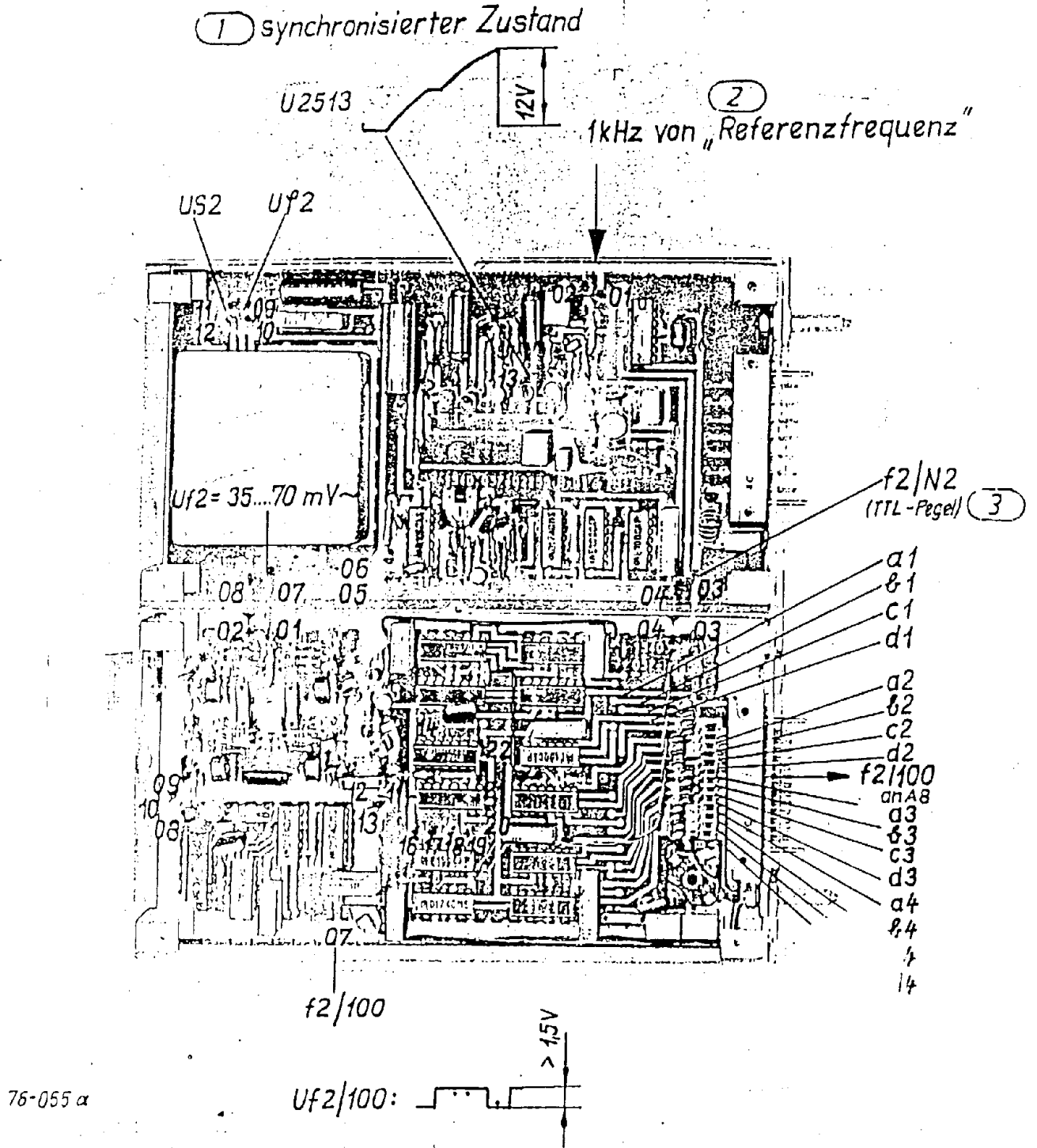
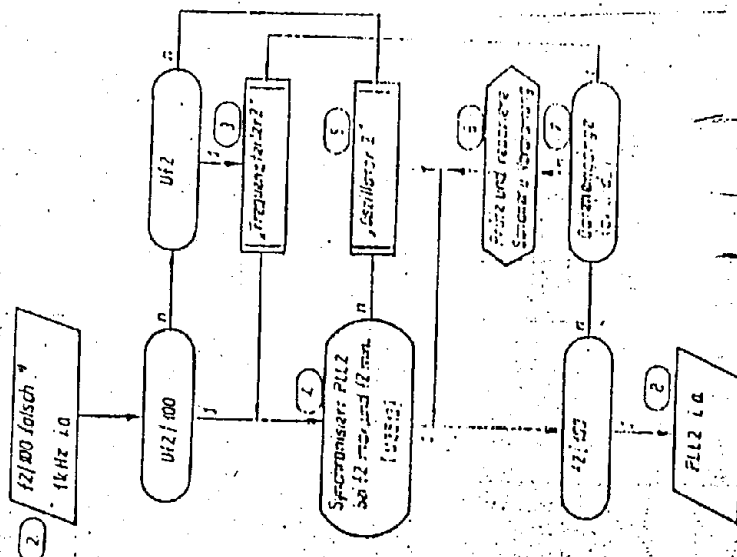


Figure 17

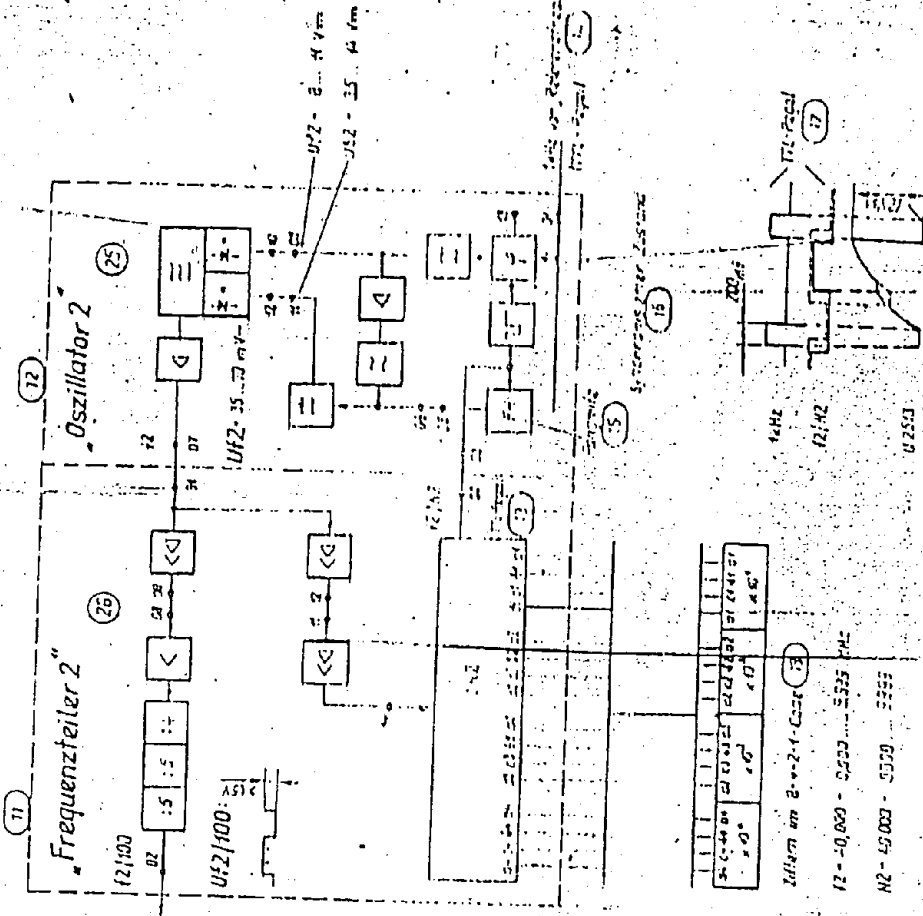
Position of test points PLL 2
19910-190.0A01

1) Prüfprogramm PLL2



- 1) falsch: - kein Ausgangssignal f2/100
 - PLL2 synchronisiert nicht
 - PLL2 synchronisiert aber Frequenz ist falsch

10) Blockschaltbild PLL2



11) Frequenzteiler 2 (PLL2)

6.3.8. Oszillator 2

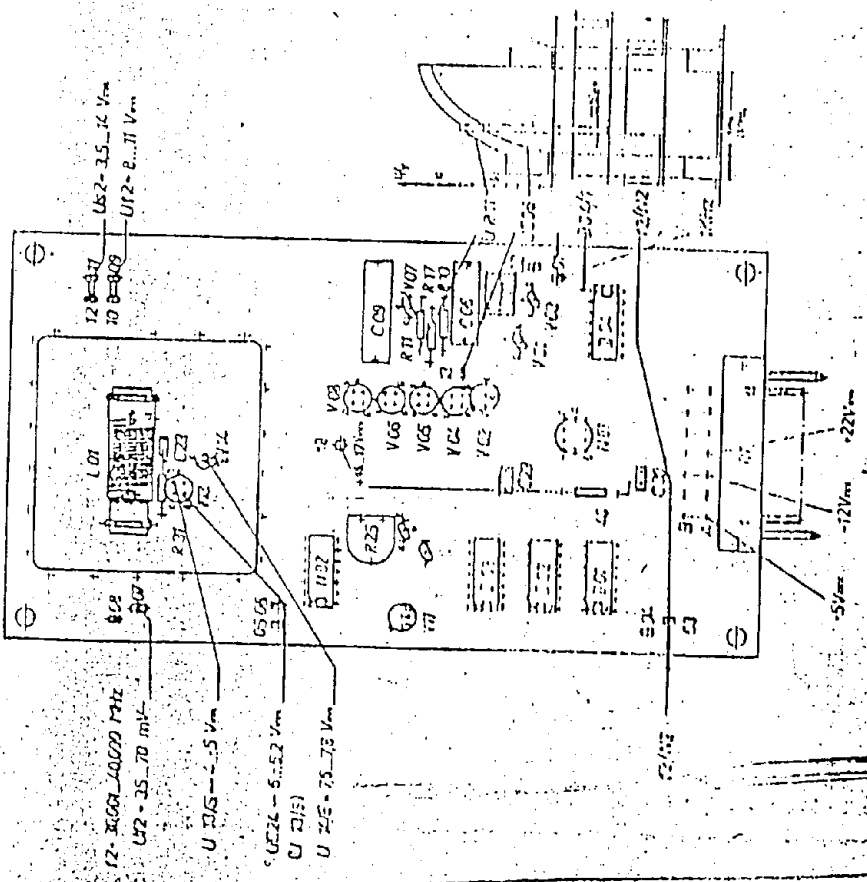
2 2 2 0 5 1 2 2 2

Koordinate Ausgangsspannung, Hz

1.	-12 V	C09
2.	-9 V	C29
3.	U72	(10)
4.	U52	(12)

Reglerrolle synchronisierfähig (1)

1. Betriebsspannungen
2. 1 kHz (R02) (01)
3. 12/12 (03)
4. U72 (10)
5. U52 (12)
6. Betrieb 11...12 Minuten, an 12 oder 10 Verschiebung, mit Frequenzstabilität v 10 kHz u. = 1 kHz synchronisierfähig
7. Frequenz und Netz Überprüfen
8. Abgleich Frequenzdivisor



No output voltage f2

- 1. -12 V 030
- 2. -9 V 029
- 3. U 2 (10)
- 4. US2 (12)

1

1. Operating voltages

- 2. 1 kHz (ref) (01)
- 3. f2/N2 (03)
- 4. U 2 (10)
- 5. U_g2 (12)

6. Open bridge 11...12, apply approx. +8 V dc to 12, synchronize with frequency switch '10 kHz' and '1 kHz'

7. Check capture aid and N 02

8. Balance phase discriminator

unter Eigentümern
Hilfsmittel oder
wird verbleibt

03

6.4.1.9. Kontrolle "Regelgleichlauf / Kanal A und B"
Automatikregelung"

- EKD: F 4 500.00 kHz, MOD 6, B 6, SEL 0, GC 1,
 df 2.00 kHz
- auf jeweils 1000 Hz-Ton im Kanal A bzw. B abstimmen.
- P4-EMK = 2 μ V ... 200 mV in 20 dB-Schritten schalten.
- Meßwert P3 (A) bzw. (B) = -3,5 dBm ... 3,5 dBm,
maximale Pegeldifferenz zwischen (A) und (B) = \pm 2 dB

6.4.1.10. Einstellen "Regelersatz Regelglied 1" (Mischer 1)

- HF-Generator P4 an Empfängereingang X 3004 (Y),
f = 4501 kHz, EMK = 100 μ V.
- ZF2 - Übergabepegel an X 3001 mit Millivoltmeter P3 messen
(über BNC-T-Stück -- Zubehör),
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 5,
 \approx ∇ mit P4 auf ca. 1000 Hz-Ton im Kanal A abstimmen.
- ZF2 - Übergabepegel - Sollwert: 5.5 \pm 0,5 mV.
- Auf GC 1 umschalten.
Mit R 3836 auf - 12 dB unter den bei GC 5 \approx ∇ von P3
angezeigten Pegelwert einstellen.

6.4.1.11. Einstellen "Trigger - Regelverstärker"

- HF-Generator P4 an Empfängereingang X 3004 (Y)
f_E 4 500.00 kHz, EMK = 1 μ V
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 2,
Mit P4 auf ca. 1000 Hz-Ton im Kanal A abstimmen
- mit Digital-Voltmeter P9 Kollektorspannung an V 3826 messen
und R 3813 so einstellen, daß U_C = V 3826 auf ca. +18 V
springt und diesen Wert beibehält.
- Zur Kontrolle: P4-EMK von 30 μ V in 10 dB-Schritten schalten.
U_C = V 3826 muß kurzzeitig < 1,5 V werden und wieder auf
ca. +18 V ansteigen.

Check of the frequency discriminator (capture aid)

D01, D02, D03, V10, V11 and V12

Open bridge 05...06

Open bridge 11...12

Apply approx. +8 V dc to 12 (suitable voltage applied to C14)

fe	f2/N2	D03		05
		Pin 9	Pin 5	
xxx 9999	> 1 kHz			< 1 V
xxx 0000	< 1 kHz			> 14 V

Check of amplifier N 02

Open bridge 05...06

Open bridge 11...12

Adjust with R 2525

$U_{pin4} \gg U_{pin5} \rightarrow U(11) < 2 V$

$U_{pin4} \ll U_{pin5} \rightarrow U(11) > 13 V$

Balancing the oscillator frequency

After replacing V 2516 or V 2517/19 (KB105B) the frequency range of the oscillator is to be checked. Balancing is performed with additional winding at L 2501-wire 0.6 mm \varnothing Cul.

- Possibilities: 2 turns in equal direction of winding
 1 turn " " "
 0 " " "
 1 turn in opposite direction of winding

fe	f2	U point 12
xxx 0000	40 0000 kHz	$\leq 14 V$ type 13 V P 8, $R_1 > 3 M\Omega$
xxx 9999	30 0001 kHz	$> 3.5 V$ type 4.5 V

x = optional setting

put on shielding cap for meas

Balancing the phase discriminator

Adjustment with R 2525

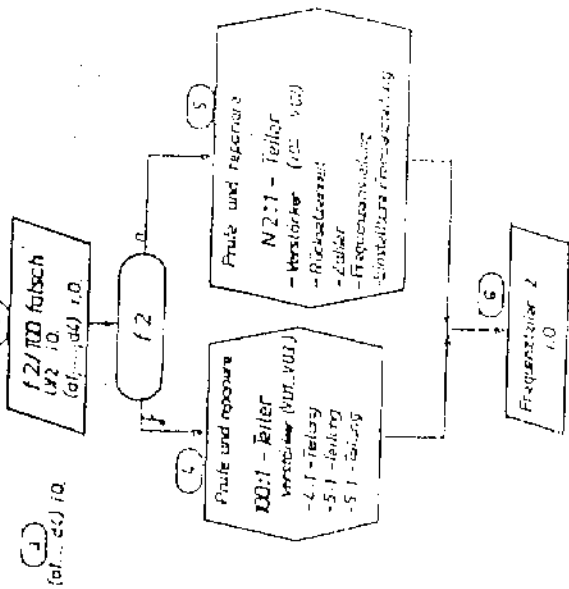
$U\varphi = 8...11 V$ at point 09 with $f_E = xxx 5000$

Observe oscillogram at C 2506 and R 25111

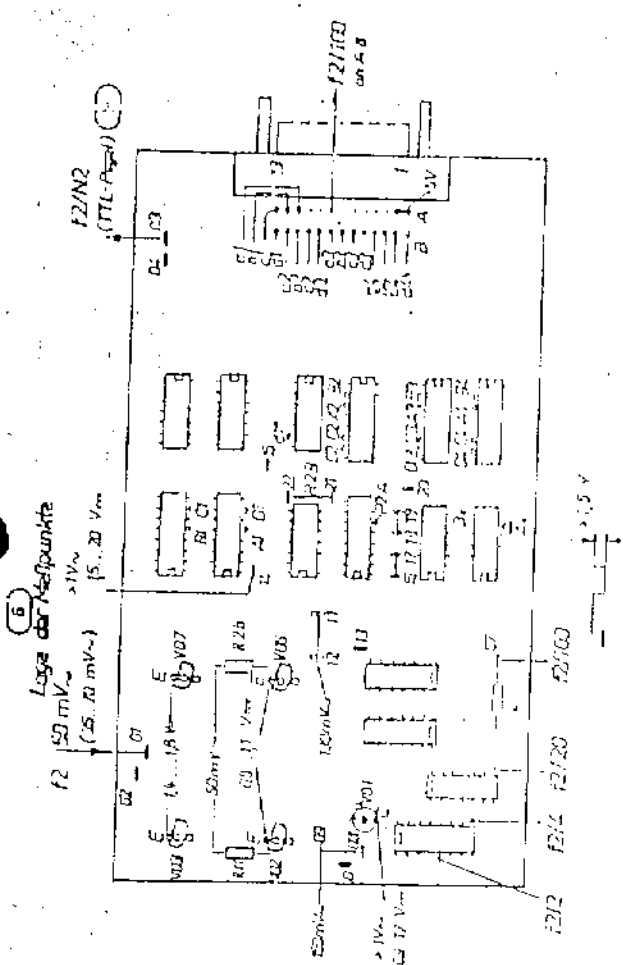
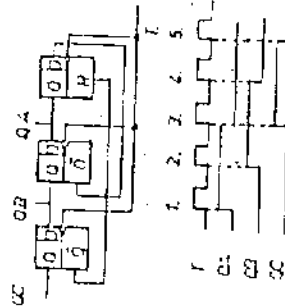
220er Eigenbau
 1/16" Umfang 20er
 1/16" wird verwendet

6.3.9. Frequency divider 2

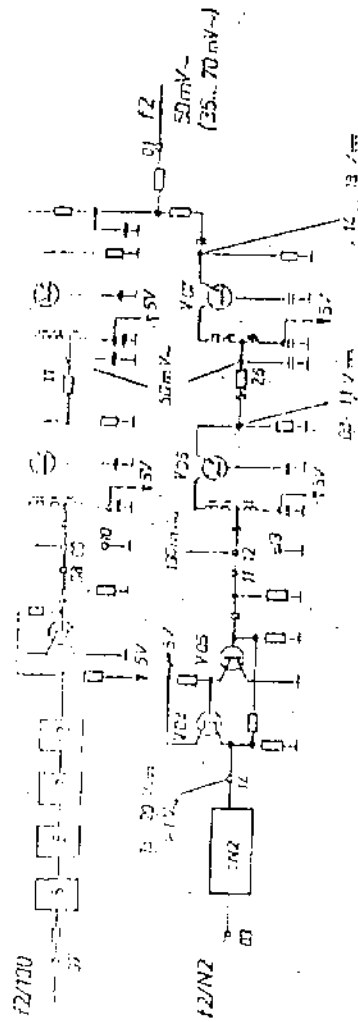
1 Prüfprogramm Frequenzteiler 2



7 Prinzip des 5:1 - Teilers

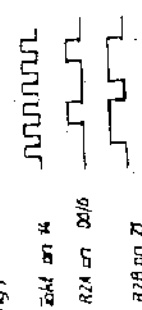


8 Verstärker A - Oszillations- und HF-Regel

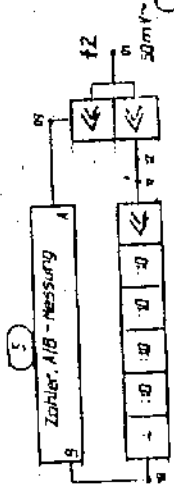


1 Prüfung des Einstellbaren Frequenzteilers 2

Rücksetzeinheit (3:1-Teilung)



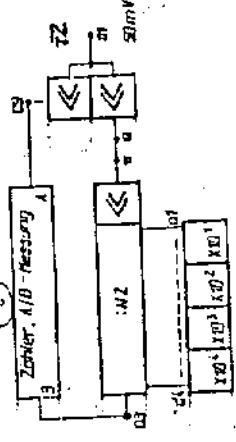
- Brücken 16-17 verbunden
- 18-19 offen
- 21-22 verbunden
- 18-17 verbunden
- 20 Hz - Schalter auf "1"
- Uf2 = 50 mV⁻
- Zähler A/5 = 40.000



- Brücken 16-17 verbunden
- 18-19 offen
- 21-22 verbunden
- 18-17 verbunden
- Uf2 = 50 mV⁻
- Frequenzeinstellung

- Brücken 16-17 verbunden
- 18-19 offen
- 21-22 verbunden
- 18-17 verbunden
- Uf2 = 50 mV⁻

Einstellbare Frequenzteilung A/B - N2 = 40.000 - (0000...9999)



- Brücken 16-17 verbunden
- 18-19 verbunden
- 21-22 verbunden
- Uf2 = 50 mV⁻

10 Einstellbarer Frequenzteiler 2

- Eingangsfrequenz f2 = 40.000 - (0.000...9999) Hz
- Ausgangsfrequenz f2/N2 = 1kHz, im Synchronisationszustand von PLL
- Teilerfaktor N2 = 40.000 - f2
- Zählerwort Zählerwort im 8+2+1+1-Code
- Zählerzeit N2 = 2000...9999
- Zählzeit N2 = 40.000
- Zählung • 40 Hz - Dekade und 2 Bit - Erzeuger siehe Blockdiagramm
- 40 Hz - Dekade und 2 Bit - Erzeuger siehe Blockdiagramm

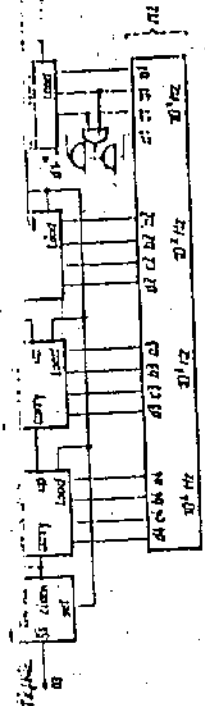
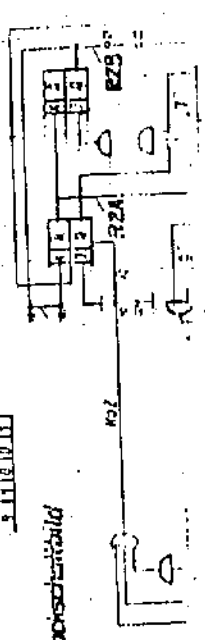
11 40 Hz - Dekade

0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9

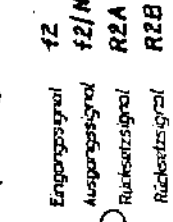
12 d1 wird umschaltet

13 2 Bit - Erzeuger

14 Blockschaltbild



15 Impulsdiagramm



3 Für die Frequenz kann man an Punkt 11 ein Signal mit einem Pegel von ca. 50 mV⁻ und einer Frequenz < 40 kHz einspeisen (P4).

6.4. Signal path (continued)

6.4.1. Check or correction of levelling

Open cassette lid (complementation side) of cassettes

'signal path 1' and 'signal path 2' and fasten outer cassettes in hinged position with cassette support (contained in the accessories).

6.4.1.1. Basic amplification 'signal path 1'

- RF generator (P4) to receiver input X 3004 (Y)

$f_p = 4\ 500\ \text{kHz}$, emf = 1 mV

- RF millivoltmeter P2 (150-mV range) via BNC-T-piece (accessories) at X 3002 (IF2 = 200 kHz)

- EKD: 4 500.00 kHz, 4, 5, 0, 5 $\approx \gamma$

- Tune with P4 to zero beat (required forward centre)

Test value P2: 50 to 60 mV

Correction: 'coarse' with R 3434 } when holding the control volume
'fine' with R 3409 } for 'signal path 1': 60 +2 dB
-1

6.4.1.2. Control volume 'signal path 1'

- Actual value from point 6.4.1.1. (test value P2) is the reference value

- $\approx \gamma$

- P4 - emf = 1 V

- Test value P2: Actual value from point 6.4.1.1. +1 dB
-2

- Correction: with R 3409

6.4.1.3. Mixer - symmetry

- receiver input X 3004 (Y) not connected

- P2 (500-mV range) to X 3002 (IF2 = 200 kHz) via BNC-T-piece (accessories)

- EKD: 0.00 kHz, 4, 5, 0, 5 $\approx \gamma$

- Test value P2 \approx 200 mV

Correction (minimization): with C 3336 (balancing capacity)

Channel A and B, manual control)

- RF generator P4 to X 0001 (casing) and via connection cable to X 3004 (plug-in).

$$f_E = 4\ 500\ \text{kHz}, \text{ emf} = 1\ \mu\text{V}$$

- AF millivoltmeter P3 and load resistance 600 ohm in parallel to line output A (25) and B (26)

- EKD: F 4 500.00 kHz, MOD 6, B 7, SEL 0, GC 5 $\approx \gamma$
 dp 2.00 kHz

- Tune with P4 to approx. 1000-Hz tone in channel B, test value P3 (B): +1 dBm, correction with R 3617 *

- Set 1000-Hz tone with rotary button (2.00-kHz step) in channel A, test value P3 (A): +1 dBm, correction with R 3855 *) maximum level fault: 0.5 dB.

6.4.1.5. Levelling 'A3E'

- RF generator P4 to receiver input X 3004 (Y)

$$f_E = 4\ 500\ \text{kHz}, \text{ emf} = 5\ \mu\text{V}, \quad m = 0.5 \quad f_{\text{mod}} = 1\ \text{kHz}$$

- AF millivoltmeter P3 in parallel to 600-ohm load resistance at AF line output A (25)

- EKD: F 4 500.00 kHz, MOD 2, B 6, SEL 0, GC 1

- Tune with P4 1000-Hz tone in channel A to minimum noise

- Balance test value P3 (A) = -1 dBm by means of R 3847 *)

6.4.1.6. Changing AF line levels (max +6 dBm)

A change of the AF line levels (up to max +6 dBm) is to be carried out with

Channel A: for A3E with R 3847

for A1A, J3E, B8E (+SB) with R 3855 (Demod. and AF)

Channel B: for B8E (-SB) with R 3617 (IF 2/B)

Cf. also Sections 6.4.1.4. and 6.4.1.5.

6.4.1.7. Balancing 'control synchronism/channel A and B, man. con

- RF generator P4, emf = 20 μV

- EKD: F 4 500.00 kHz, MOD 6, B 6, SEL 0, GC 5

- Tune to 1000-Hz tone in channel A or B

- Adjust test value P3 (B) = 0 dBm with $\approx \gamma$

- Adjust test value P3 (A) = 0 dBm \pm 0.5 dB with R 3734

- Switch P4-- emf = 2 μV in 20-dB steps and set test value P3 (B) = 0 dBm with $\approx \gamma$

- Maximum level difference between (A) and (B): \leq 1.5 dB

*) For increased AF output level (e.g. + 6 dBm) balance to a value being 6 dB higher

4.1.8. Balancing 'automatic control/channel A and B'

RF generator P4, emf = 200 mV
 EKD: F 4 500.00 kHz, MOD 6, B 7, SEL 0, GC 1, df 2.00 kHz. Tune with P4 to approx. 1000-Hz tone in channel B, set measuring value P3 (B) = +2 dBm with R 3616
 Set 1000-Hz tone with rotary button \approx (2.00-kHz step) in channel A
 Set test value P3 (A) = +2 dBm with R 3801, max. level fault: 0.5 dB
 P4-emf = 2 μ V, test values P3 (A) or (B) = -2 dBm ... 0 dBm

4.1.9. Check 'control synchronism/channel A and B, automatic control'

EKD: F 4 500.00 kHz, MOD 6, B 6, SEL 0, GC 1, df 2.00 kHz
 Tune to 1000-Hz tone in channel A or B
 Switch P4 - emf = 2 μ V ... 200 mV in 20-dB steps
 test values P3 (A) or (B) = -3.5 dBm ... 3.5 dBm,
 maximum level difference between (A) and (B): \leq 2 dB

4.1.10. Adjustment 'control start/control element 1' (mixer 1)

RF generator P4 to receiver input X 3004 (Y), f = 4501 kHz,
 emf = 100 μ V
 IF 2 - interposition level on X 3001 to be measured with millivoltmeter P3 (via BNC-T-element - accessories).
 EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 5,
 Tune \approx with P4 to approx. 1000 Hz-tone in channel A
 IF 2 - interposition level - rated value : 5.5 ± 0.5 mV
 Switch over to GC 1
 Adjust to a value -12 dB below the one read by P3 for GC 5 \approx with R 3836.

4.1.11. Adjustment 'trigger - control amplifier'

RF generator P4 at receiver input X 3004 (Y)
 f = 4 500.00 kHz, emf = 1 μ V
 EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 2
 Tune with P4 to approx. 1000-Hz tone in channel A
 Measure with digital voltmeter P9 collector voltage at V 3826 and adjust R 3813 such that $U_C = V 3826$ jumps to approx. +18 V and maintains this value.
 For checking: Switch P4 - emf from 30 μ V to 1 μ V in 10-dB steps. U_C shall decrease for a short time to < 1.5 V and increase then again to approx. +18 V.

Manual & and manual GENERAL

- RF generator P4 to receiver input X 3004 (Y)
- $f_E = 4\,500\text{ kHz}, \text{ emf} = 30\ \mu\text{V}$
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 1
- Tune with P4 to approx. 1000-Hz tone in channel A
- Measure with digital voltmeter P9 capacitor voltage C 3808
- Measure with P9 the voltage at slider of R 3829 and adjust with R 3829 to a value that is 0.5 V below $U_C\ 3808$ (guide value: $4.3\ \text{V} - 0.5\ \text{V} = 3.8\ \text{V}$)

6.4.1.13. Balancing 'display E γ ' (LED row and decimal digital display)

- RF generator P4 to receiver input X 3004 (Y)
- $f_E = 4\,500\text{ kHz}, \text{ emf} = 1\ \text{mV}$
- EKD: F 4 500.00 kHz, MOD 4, B 2, SEL 0, GC 1, TEST 3
- Changeover switch 'LED row' (2) \rightarrow E γ
- Tune P4 to zero beat (IF forward centre)
- Balance the emf pairs in the sequence 30 μV , 30 mV and 3 μV and 1 V with the assigned preset controllers R 45145 ... R 45148 to the values 'decimal digital display' given in the table below.

	P4 - emf			
	30 μV	30 mV	3 μV	1 V
LED row	30 dB (μV)	90 dB (μV)	10 dB (μV)	120 dB (μV)
Decimal digital display	15 ± 1	45 ± 1	5 ± 1	60 ± 1
Preset controller	R 45145	R 45146	R 45148	R 45147

(Position of preset controller cf. Figure 1)

Note: dB (μV) = dB exceeding 1 μV i.e., 0 dB (μV)

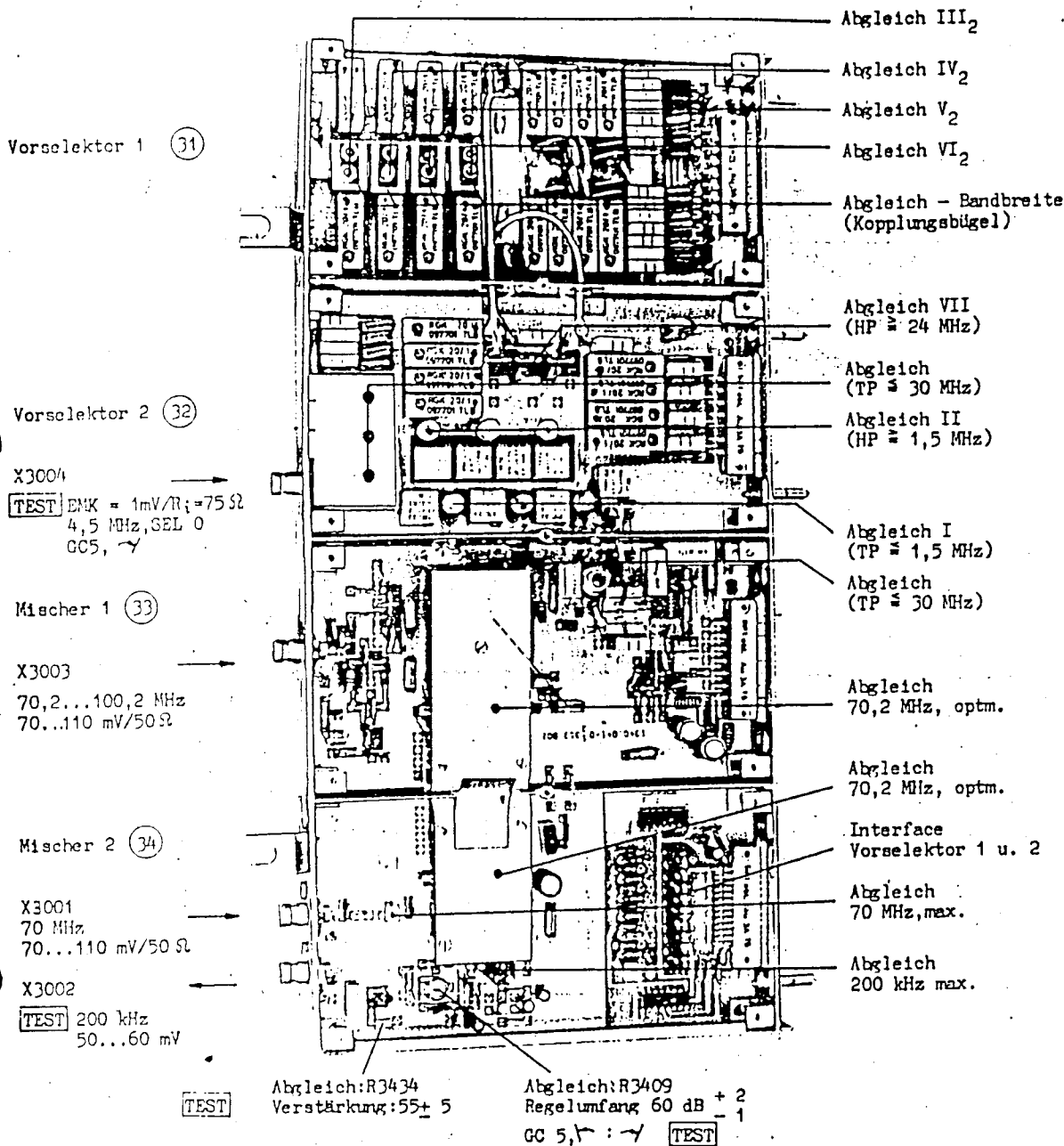
If rated balancing cannot be achieved: change shift register R 45122 (150 kohm ... 220 kohm)

dB (μV) = dB over 1 μV , i.e. 0 dB (μV) = 1 μV

100% Kopiergenau
 fädigste Qualität
 mita verteilt

100% Kopiergenau
 fädigste Qualität
 mita verteilt

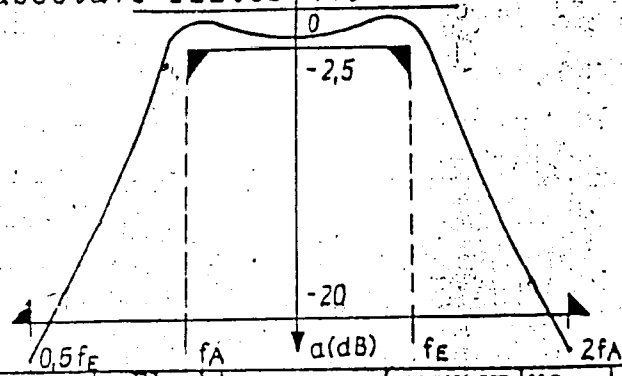
The following section provides hints on troubleshooting in the cassette 'signal path 1'.
 For this purpose, the plug-in is to be connected outside the casing via adapter cable (30- and 8-core cable, contained in the accessories).
 For fault localization: : dismount cassette lid (complementation side)
 . perform level check according to the figure



86-033 a

Figure 18
 Signal path 1 1340.041-01311

6.4.2.1.1. - Selectivity characteristics 'preselector 1'
 (Switchable suboctave filter 1.5 MHz to 24 MHz in 12 subranges)



	Pass range (≤ 2 dB) $f_A \dots f_E$ (MHz)	Blocking range (mean value ≤ 20 dB)		Balancing frequency	Balancing elements
		$\leq 0.5 \cdot f_E$ (MHz)	$\leq 2 \cdot f_A$ (MHz)		
III 1	1.5 ... 2	≤ 1	≤ 3	-	-
III 2	2 ... 2.5	≤ 1.25	≤ 4	2.25 MHz	L3101, L3102
III 3	2.5 ... 3	≤ 1.5	≤ 5	-	-
IV 1	3 ... 4	≤ 2	≤ 6	-	-
IV 2	4 ... 5	≤ 2.5	≤ 8	4.5 MHz	L3103, L3104
IV 3	5 ... 6	≤ 3	≤ 10	-	-
V 1	6 ... 8	≤ 4	≤ 12	-	-
V 2	8 ... 10	≤ 5	≤ 16	9 MHz	L3105, L3106
V 3	10 ... 12	≤ 6	≤ 20	-	-
VI 1	12 ... 16	≤ 8	≤ 24	-	-
VI 2	16 ... 20	≤ 10	≤ 32	18 MHz	L3107, L3108
VI 3	20 ... 24	≤ 12	≤ 40	-	-

Each subrange ends at $f_E - 10$ Hz
 - For all measurements $Z_E = Z_A = 75$ ohm
 - Balancing with broad-band wobble measuring set-up (P7)* between cassette input X 3004 and preselector 2 output P 3205.

*) When balancing with RF generator (P4), attenuate the coil that is not to be balanced with a 300-ohm resistance.
 - For balancing: Remove connection to mixer 1 (P 3205 \rightarrow P 3301) at P 3205: 75-ohm resistance \rightarrow \perp

unter Erhalten
 Wahrung der
 wird verfolgt.

For switching on the subrange to be balanced:

- EKD: for range III 2: F 2250.00, SEL 1
- range IV 2: " 4500.00, " 1
- range V 2: " 9000.00, " 1
- range VI 2: " 18000.00, " 1

- Coil balancing according to set-point value-selectivity characteristics

Adjust with strap to insertion loss of ≈ 2.5 dB at the pass-range limits f_A and f_E with adherence to the selection ratings at $0.5 \cdot f_E$ and $2 \cdot f_A$.

- In the other subranges (III 1 ... VI 1 and III 3 ... VI 3):
Check insertion loss ≤ 3 dB and selection ratings according to 6.4.2.1.1.

84

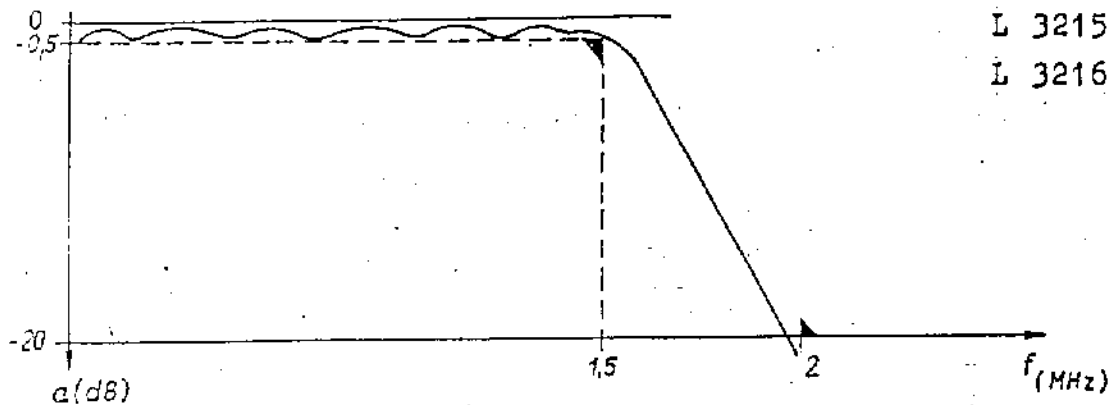
Range I LP \approx 1.5 MHz

Balancing elements

L 3214

L 3215

L 3216



Range II HP \approx 1.5 MHz LP \approx 30 MHz

LP \approx 30 MHz

Balancing elements

L 3217

L 3218

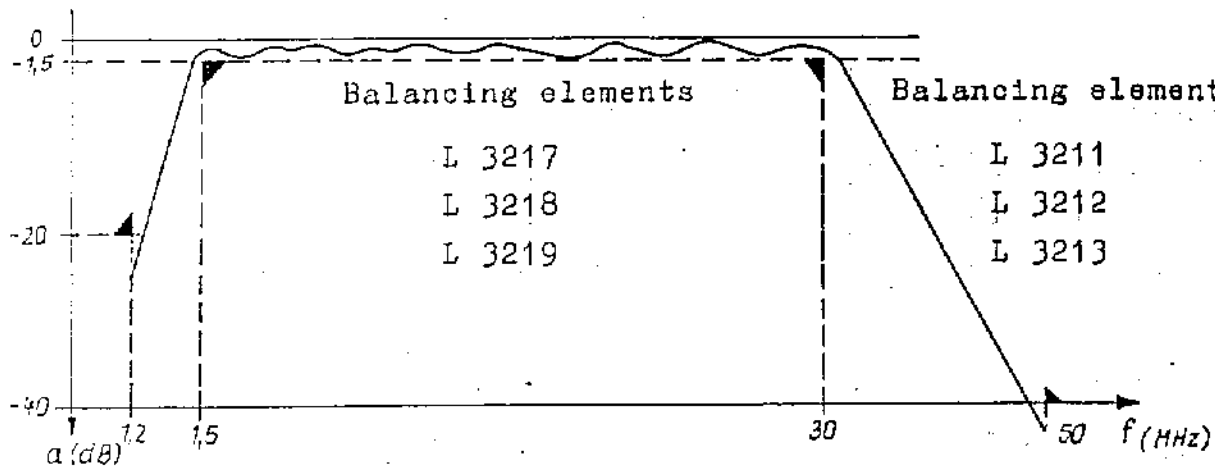
L 3219

Balancing elements

L 3211

L 3212

L 3213



Range VII HP \approx 24 MHz LP \approx 30 MHz

LP \approx 30 MHz

Balancing elements

L 3220

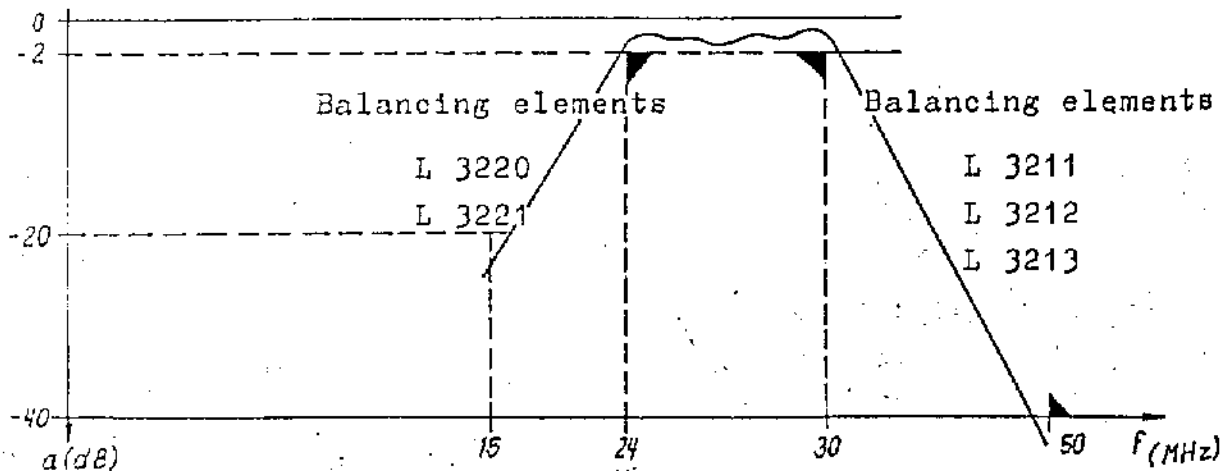
L 3221

Balancing elements

L 3211

L 3212

L 3213



- For all measurements $Z_E = Z_A = 75 \text{ ohm}$
- Balancing with broad-band wobble measuring set-up (P7) between: cassette input X 3004 and preselector 2 - output P 3205
- When balancing: Remove connection to mixer 1 (P 3205 \rightarrow P 3301) at P 3205: 75-ohm resistance $\rightarrow \perp$
- For balancing the respective preselection range the following operation of the receiver is required:

For range: I : BKD: F 250.00 kHz, SEL 1
 " II : BKD: " 4500.00 kHz, " 0
 " VII : BKD: " 26000.00 kHz, " 1

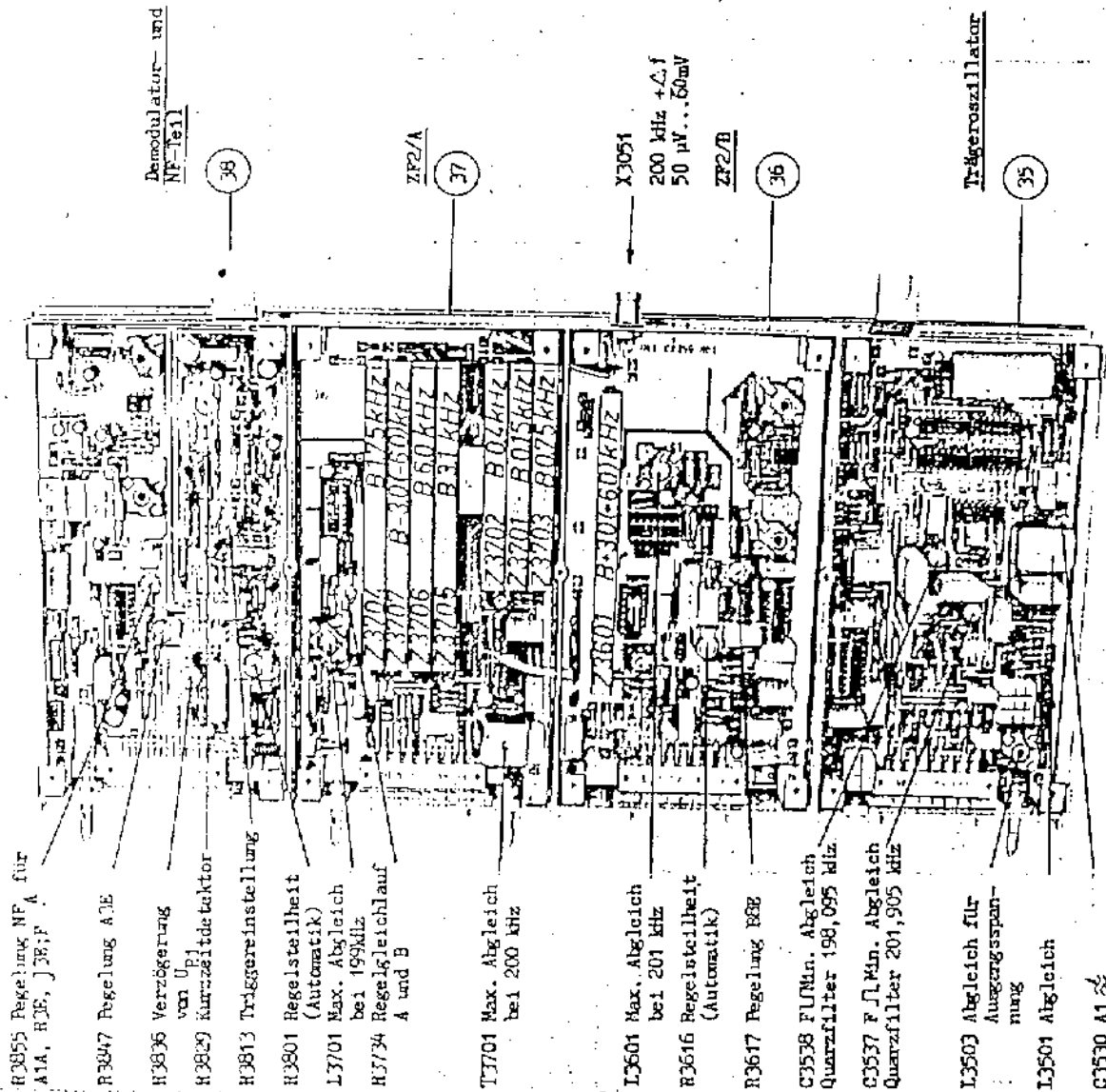
6.4.3. Signal path 2 1340.041-01321

The following section supplies hints on troubleshooting in the cassette 'signal path 2'.

For this purpose, the plug-in is to be connected outside the casing via adapter cable (30-and 8-core cable, contained in the accessories).

For fault localization:

- . Dismount cassette lid (complementation side)
- . Apply input signal from NF generator (P4) to X 3051 (input socket for signal path 2)
- . Load line output A (25) and line output B (26) at one end — 1 and with R = 600 ohm to avoid interferences
- . Perform level check acc. to figure 19 or 20.



86-0340


Figure 19
Signal path 2 1340.041-01321

Pegelkontrollen bzw. Pegelkorrektur


	HP-Generator (74)		Sendeleist.	Bandbreite	Verst. Regelung	Prüfung	Prüfpunkt	Messwerte	
	f	U _e						U _{best.}	U _{max.}
OC 5 U _{ZP2} -Verst. U _{f₂} -Verst. U _{f₂} -Kont.	-	-	MOD 1	B 5	OC 5	Kontrolle U _{best.} U _{max.}	X 3801 /B11	199 mV	U _{best.} U _{max.} 0,75 V 0,3 V
	199 kHz	55 µV	-	-	OC 5	I 3701 Max.	ZP2 - Ausgang (27)	200 mV	> 100 mV
	200 kHz	10 µV	MOD 3	-	-	T 3701 Max.	ZP2/B P 3605	200 mV	> 30 mV Leuchtbild
Drehoszillator (U _{f₂} , f ₂)	-	-	MOD 1	beliebig ausw.	-	Kontrolle	X 3801 /B2	199,8 kHz 199,5 kHz	110...160 mV
	200 kHz	-	MOD 3		Kontrolle f und U _e	-	-	200,00 kHz	120...170 mV
	-	-	MOD 4		-	-	-	200,00 kHz	-
Regelung/323 UR/1A1	-	-	MOD 5	-	-	-	-	-	-
	Regelung/323	55 mV	MOD 4	B 16	OC 5	R 3895 einstellen	NP-Lage-Ausg.	1 kHz	0 dB
	Regelstell- wert (Autosensit.)	110 µV	-	-	OC 1	R 3801 einstellen Kontrolle f, U _e	-	1 kHz	-1 dB
	Regelstwert U _{f₁}	25 mV	-	-	-	R 3836 einstellen	-	1 kHz	-1,2 dB
	Pegelung/A33 U _{mf} (A)	1,5 mV	-	-	-	R 3847 einstellen	X 3801 /B10 NP-Lage-Ausg. A	1 kHz	12,5 V
	Abbrück- stärker	1 mV	MOD 2	-	-	-	-	1 kHz	-1 dB
Pegelung/368 U _{mf} (B)	1,5 mV	-	MOD 4	-	OC 5	Kontrolle □ est.	-	1 kHz	± 2 V _{eff} B Obs
	55 µV	55 µV	MOD 6	B 7	OC 5	I 3601 Max. R 3617 einstellen	NP-Lage-Ausg. B	1 kHz	0 dB

Figure 20



0 wird vertrieben

Main characteristics are values and frequency response of the output voltage U_A as well as the function of the LED V 4602 

Test and troubleshooting are accomplished in the sequence "Value of the output voltage" - "Frequency of the output voltage".

The tables (figure 21, 22) show, in dependence on the class of emission (MOD) selected, the voltage U of the functional groups or the voltages and frequencies at the inputs U_E, f_E and at the output $U_A, f_A (\hat{=} f_{U3})$ as well as the function of the LED V 4602 

6.4.3.1.1. Output voltage and control voltage generator

The maximum balancing L 3503 is performed at A1A (very flat maximum) or at F  alternating with F  to the equal value of U_A . The crystal oscillator is amplitude-controlled via T 3514.

6.4.3.1.2. Crystal oscillator

The crystal-stabilized oscillator is tuned at its frequency by means of the parallel circuit L 3501-C 3521, C 3530 and the capacity diode V 3529.

The frequency range is balanced at A1A with C 3530 (coarse) and L 3501 (fine) to $f_A = 198.8$ kHz with 0 V at X 3501/B7 and $f_A = 199.5$ kHz with 9.5 V at X 3501/B7.

Access to the balancing core of L 3501 is provided after dissoldering of the metal tip in the cap centre. After accomplishing balancing work the coil is to be covered again with the metal tip.

6.4.3.1.3. Store and switch

The switch is actuated by the trigger.

Class of emission R3E, $U_E = 200$ mV, $f_E = 200$ kHz $\pm \Delta f_E$.

The switch is closed as V 3523 and V 3526 are blocking and V 3508 or V 3509 cause opening - depending on the potential difference - between emitter and collector thus closing the phase control loop

$$\Delta f_A = \Delta f_E.$$

90

Class of emission R3E, $U_E = 50$ mV, $f_E = 200$ kHz $\pm \Delta f_E$.

The switch is open because V 3508 and V 3509 are blocking via V 3521.
The phase control loop is open, Δf_A is independent of Δf_E , f_A is nearly constant and changes with -3 Hz/min (discharge of store capacitor C 3518).

In case f_A is dependant on f_E : check V 3523, V 3526, V 3508, and V 3509.

When change of f_A too large: replace T 3508, T 3509, T 3510, T 3525, C 3518 in this sequence.

Attention! V 3510 is a MOS transistor. When changing V 3510 or any components which are fed to its transistor terminals these are to be shortened.

In the class of emission J3E, $U_E = 200$ mV, $f_E = 200.000$ kHz the operating condition R3E is equal to $U_E = 200$ mV, $f_E = 200.000$ kHz. The inverse voltages for V 3523 and V 3526 are firmly switched on via V 3540.

6.4.3.1.4. Phase detector

Direct voltage to N 3501/8 at $U_E = 0$: approx. 6 V.

With the control loop closed the voltage at N 3501/8 varies irregularly by approx. ± 10 % (phase jumps of f_A).

6.4.3.1.5. Voltage path 200.000 kHz

Characteristic of the voltage path: V3501/B3-R3506-V3516-R3503-N3501/14

6.4.3.1.6. Voltage path 200 kHz + Δf_E

Characteristic of the voltage path: V3501-R3508-V3518-C3505-R3503-N3501/14

6.4.3.1.7. Amplifier and trigger

Gate D 3504/9, 10, 11, 8 is included in the amplifier. E 3520 causes slow recharging of C 3517 after having applied the input voltage and with this the delayed response of the trigger (0.5 s). $U_E \cong 200$ V 3504C 15.5 V \rightarrow 5 V; V 3503E 3.5 V \rightarrow 13.5 V.

V 3521 provokes quick recharging of C 3517 after disconnection of the input voltage and thus immediate response of the trigger.

6.4.3.1.8. Divider 200 kHz/1.905 kHz

Divider ratio 1:105.

In the classes of emission F the divider is put into operation via K input D 3503/10 by applying 2.7 V. The divider consists of the counter components D 3501 and D 3502 as well as of the decoding circuit D 3504 (2 gates) and D 3503 for releasing a reset pulse. Every 103rd pulse at D 3501/14 causes that H potential is applied to the J inputs of D 3503. Thus, the 104th pulse can release a reset pulse at the Q output. This pulse is terminated with the trailing edge of the 105th pulse.

6.4.3.1.9. Mixer 200 kHz \pm 1.905 kHz

The summation and difference frequencies are available opposite in phase at the outputs N 3502/12 and N 3502/13.

Input voltages: N 3502/6.14 approx. 2 V; N 3502/7.9 approx. 3.6 V.

A summation voltage of approx. 400 mV is applied to N 3502/12, 13 (both input- and mixed frequencies).

6.4.3.1.10. Crystal filter 201.905 kHz and 198.095 kHz

Both crystal filters are bridge filters whose branches are activated opposite in phase by N 3502/12 or N 3502/13. After crystal exchange a maximum balance von U_A by minimum tuning of the crystal frequency with C 3535 or C 3536 may be required.

C 3537 and C 3538 provide minimum balancing of the distortion products of U_A (suppression of the undesired frequencies).

Table

DC voltages of the function groups in dependence of the class of emission selected (MOD)

Test value	Function group	Test point	A1A	A3E	R3E, B, SE	J3E, BSE	F0, F 11	F 11
Output amplifier and control voltage generator	Crystal oscillator	X3501/B7	0...9.5	0	0	0	0	0
			A1 pitch control	0	0	0	0	0
Store and switch	Phase detector	V3542/K	0	0	16.5	16.5	0	0
			V3519/K	0	0	16.5	16.0	0
DC voltages of the function groups	Voltage path	200.000 kHz	0	0	0	0.7	0.7	0.7
			200 kHz ± Δf	0	0	0.7	0	0
D (V)	Amplifier and trigger	V3546/K	0	0	16.0	(5)	16	16
			Divider 200/11.905 MHz	5	5	5	5	5
D (V)	Mixer 200 kHz + 1.905 MHz	X3501/A1 D3503/10	0	0	0	0	2.7	2.7
			V3534/K	0	0	0	0	16.5
D (V)	Crystal filter	201.905 MHz	0	0	0	0	17.5	0
			198.095 MHz	0	0	0	0	0
		X3501/A9	0	0	0	0	0	
		X3501/411	0	0	0	0	0	

Table

Voltages and frequencies at the inputs and at the output as well as the function of the carrier display in dependence on the class of emission selected (MOD)

Test value	Function group	Connection points	A1A	A3E	R3E, R _E EE	J3E, JEE	F0, FΠ	FU
Input voltages and frequencies (test)	Voltage path 200.000 kHz	X3501/B3 — X3501/A3 ⊥	—	—	—	200 mV	200 mV	200 mV
						200.00 kHz	200.00 kHz	200.00 kHz
Output voltages and frequencies	Voltage path 200 kHz + Δf _E	P3501 — P3502 ⊥	—	—	50mV/200mV 200kHz+Δf _E Δf _E ≈ 50Hz	—	—	—
					Output amplifier	110 mV to 160 mV	0	120 to 170 mV
R _A = 680 ohm	f _A f _{U3}	X3501/B13 X3501/A13	< 198.8 to > 199.5 kHz (A1-pitch control)	—	200kHz+Δf _A U _E =200mV Δf _A =Δf _E U _E =50mV Δf _A const. (~3Hz/min)	200.000 kHz f _A =f _E	201.905 kHz	198.095 kHz
			Trigger	dark	dark	U _E =200mV lit U _E =50mV dark	dark	dark

Figure 22

6.4.3.2.1. Amplification in signal path 2 (X3051 — P3705)

$U_e = 55 \mu V$ at X3051 (RF generator P4), GC 5 and $\approx \rightarrow$

$U_a = 100 \text{ mV to } 200 \text{ mV}$ at P3705 — \perp (millivoltmeter P3)

$U_{R2} = 0.75 \text{ V}$

Amplification difference with bandwidths B 2... B 4 : $\approx 4 \text{ dB}$
with B 1 : $\approx 6 \text{ dB}$

Attention Exchange IF2 amplifier circuits N3603 (IF2/B) and N3702 (IF2/A) only in pairs (spare part in B1)

6.4.3.2.2. Carrier amplifier (for R3E and B_R8E)

200 kHz/ $U_e = 10 \mu V$ at X3051 (RF generator P4)

$U_a = 30 \text{ mV to } 100 \text{ mV}$ at P3605 — \perp (millivoltmeter P3)

3 dB bandwidth : $\approx \pm 50 \text{ Hz}$

6.4.3.2.3. Bandwidth and selection of mechanic filters

B	Rated bandwidth	3 dB bandwidth	60 dB bandwidth
1	0.15 kHz	$\approx \pm 50 \text{ Hz}$	$\approx \pm 250 \text{ Hz}$
2	0.4 kHz	$\approx \pm 150 \text{ Hz}$	$\approx \pm 500 \text{ Hz}$
3	0.75 kHz	$\approx \pm 300 \text{ Hz}$	$\approx \pm 850 \text{ Hz}$
4	1.75 kHz	$\approx \pm 750 \text{ Hz}$	$\approx \pm 1250 \text{ Hz}$
5	3.1 kHz	$\approx \pm 1.5 \text{ kHz}$	$\approx \pm 2.15 \text{ kHz}$
6	6.0 kHz	$\approx \pm 3.0 \text{ kHz}$	$\approx \pm 4.0 \text{ kHz}$
7*)	+3.0 kHz	$\approx +(0.25...3.0) \text{ kHz}$	$\approx -0.25 \text{ kHz}; \approx +3.5 \text{ kHz}$
**)	+6.0 kHz	$\approx +(0.3...5.9) \text{ kHz}$	$\approx -0.3 \text{ kHz}; \approx +6.8 \text{ kHz}$
8*)	-3.0 kHz	$\approx -(0.25...3.0) \text{ kHz}$	$\approx +0.25 \text{ kHz}; \approx -3.5 \text{ kHz}$
**)	-6.0 kHz	$\approx -(0.3...5.9) \text{ kHz}$	$\approx +0.3 \text{ kHz}; \approx -6.8 \text{ kHz}$
9		signal path blocked	

*) EKD 511

***) EKD 512

Attention The signs of the built-in sideband channel filters are opposite to that of the input signal (sideband commutation in mixer 1).

Lucas Eigentum
Hilfjung sein
ist eine Pflicht

1 wird verifiziert

6.4.3.3. Demodulator and AF section 1340.039-01358

6.4.3.3.1. Demodulator/A1A; J3E; F1B; F3C

Level outline with input signal applied

At P 3801 → ⊥ : IF2 signal = 201 kHz or 200 kHz/100 mV, GC 5

At N 3801/14 : $U_{\text{carrier}} (\text{lim.}) = 200 \text{ mV to } 350 \text{ mV}_{\text{ss}}$

At N 3801/9 : $U_{\text{IF2}} = 7 \dots 15 \text{ mV} \approx$

At N 3801/8 : $U_{\text{AF}} = 50 \dots 55 \text{ mV} \approx$

adjust with R 3855

6.4.3.3.2. Demodulator/A3E

Level outline with input signal applied

At P01 → ⊥ : IF2 signal = 200 kHz/m = 0.5; 1 kHz, 100 mV, GC 5

At X01/14 : IF2 signal = 3 ... 5 mV \approx

At X01/8 : $U_{\text{AF}} = 50 \dots 55 \text{ mV} \approx$; adjust with R 3847

Attention At input P 3801 → ⊥ : approx. 1.1 V dc voltage

6.4.3.3.3. AF line amplifier 'channel A'

Level outline with input signal applied

At N 3802/3 : $U_{\text{AF}} = 50 \dots 55 \text{ mV} \approx$


At N 3802/6 : $U_{\text{AF}} = 0.775 \text{ V} \approx$ (with 52 mV at N 3801/8)

At X 3801/B4 : $U_{\text{AF}} = 0.775 \text{ V} \approx$

Line output 'A' : at X 3802/5 : 8.8 ... 9.2 V ==

at X3802/10 : 8.8 ... 9.2 V ==

6.4.3.3.4. Monitoring amplifier

U_{B} at X X 3801: 100 mV (for 0.5 W across 8 ohm X 1021  external)

(Correcting of amplification possible with R 71.)

Attention Do not generate AF power with the heat radiator disconnected (thermal overload) !

6.4.3.3.5. Control amplifier

- Manual control: GC 5

Generation of U manual control by voltage divider

R 3845, R 1002 (\approx) and R 1007

R 1002	→ Mixer 1	→ IF amplification A/B
γ	$U_{R1} \approx 14.5 \text{ V} \approx$	$U_{R2} \approx 0.75 \text{ V} \approx$
γ	$U_{R1} \approx 9.5 \text{ V} \approx$	$U_{R2} \approx 0.3 \text{ V} \approx$

- Automatic control: GC 1, GC 2

At P 3801 → \perp : $U \approx = 100 \text{ mV}/200 \text{ kHz}$

At IF output (27): $\approx 100 \text{ mV}$ (without load)

U at V 3821_B = approx. 45 mV \approx (adjustable with R 3801)

Control detector/A : U at V 3824_B > +4 V

	Trigger (not driven)	Trigger (driven)
Trigger V 3826 _C	$\approx 0.55 \text{ V} \approx$	$> 17 \text{ V} \approx$
Holding circuit V 3827 _C	approx. 1,25 V \approx	approx. 0.25 V \approx
Long-time detector V 3828 _B	approx. 0.66 V \approx	0

$U_C 3808 = ,3 \dots 4 \text{ V}$

Short-time detector $U_{R3829/R3830} = 3 \dots 4 \text{ V} \approx$

Amplifier V 3829_B , $= 13 \dots 14 \text{ V} \approx$

Amplifier V 3830_C $= 12 \dots 13 \text{ V} \approx$

Voltage of slider R 29 = $U_C 3808 - 0.6 \text{ V}$

Dieser Eigenton
 freiliegend oder
 nicht verfügbar.

Freiliegend oder
 nicht verfügbar.

6.5. PLL demodulator 1340.041-01258

6.5.1. Check 'input signal' (X 2801/A, B1 or X 0002)

Receiver setting: F 0,00 kHz

B 6

MOD 7, 8 or 9

GC 5

Adjust input voltage with control " \approx " to 0.8 V.

Measure input frequency at MOD 7, 8 and 9

Setpoint value: 1905 Hz \pm 1 Hz

6.5.2. Check 'input band-pass' (N 2801)

(P 12 serves as earth reference for all measurements on this pc board.)

Measure 3-dB decrease at P 01 with $\Delta F = 0.10$ kHz

Pass range approx. 1.1 kHz to 2.7 kHz

Slope steepness approx. 12 dB/oct.

Operating residual attenuation 1.5 dB to 2 dB

6.5.3. Check 'limiter amplifier' (W 2802, V 2804, V 2805)

U_{P02} : approx. V_{rms} at $U_e = 500$ mV to 2.5 V

(adjust with control \approx)

U_{P03} : approx. 0.8 V_{pp}

6.5.4. Check 'PLL' (N 2803, N 2804, D 2801, V 2806 ... V 2816)

Measure PLL zero position and VCO frequency with the signal path blocked (B 9).

Rebalancing: PLL zero position with R 2826 (0 V \pm 5 mV at P04)

VCO frequency with R 2842 (1905 Hz \pm 2 Hz at P05)

(Forced changeover with IF bandwidth B)

100-Bd low pass: at B 1, 2, 3 (f_g approx. 150 Hz)

600-Bd low pass: at B 4, 5, 6 (f_g approx. 900 Hz)

Offset correction : for 100-Bd low pass with R2867 at P 09
for 600-Bd low pass with R2876 and R2883
at P 08 and P 09

6.5.6. Check 'amplifier' (N 2810)

Measure $V =$ approx. 40 with low Δf (e.g. 80 Hz)

Offset correction with R 2891.

6.5.7. Check 'evaluator circuit' (N 2811)

At centre frequency (1905 Hz)

: $U_{P11} = 0 V \pm 15 mV$

At centre frequency $+\Delta f = 500$ Hz

: $U_{P11} = + 1 V \pm 50 mV$

At centre frequency $-\Delta f = 500$ Hz

: $U_{P11} = - 1 V \pm 50 mV$

In case of exceeding U_{P11} values

: balance with R 2892

In case of too low U_{P11} values

: balance with R 2897

6.5.8. Check 'Line current for teleprinter'

Connect ammeter with 200 ohm (load resistance) in series to teleprinter terminal (X 0008, 3 and 4).

At MOD 1 ... 7 : 40 mA \pm 5 mA (correction with R 28106)

6.5.9. Check 'holding and capture range of PLL'

Receiver setting: F 0.00 kHz

dF 0.01 kHz

MOD 8 and 9

B 6

GC 1

Changeover switch 'LED row' (2) \rightarrow ' $\Delta f \times 2$ '

Dieser Gegenstand ist Eigentum der Bundespost und darf nicht ohne Genehmigung der Bundespost veröffentlicht werden.

Holding range: Setpoint value: $\Delta f \approx \pm 900$ Hz referred to centre frequency

Increase frequency with rotary button " \approx " until luminous point of the LED row jumps from row end to row centre.

Capture range: Setpoint value: $\Delta f \approx \pm 800$ Hz referred to centre frequency

Detune frequency of Δf values 2.00 kHz towards 0.00 kHz by means of rotary button " \approx ".

accomplish this function check at MOD 8 and MOD 9.

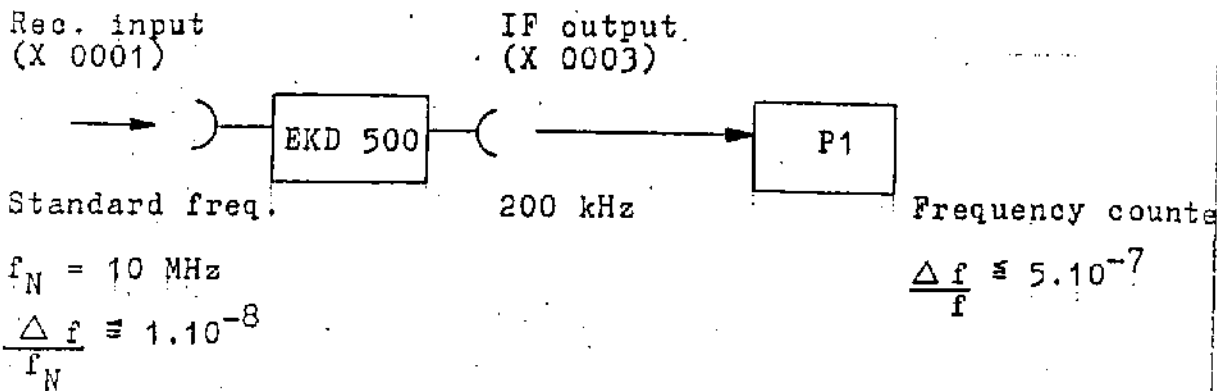
check simultaneously the synchronization process through monitoring tone.

100

7.1. Frequency accuracy

7.1.1. Measuring and correcting with standard test conditions

Temperature +15 °C to +35 °C
 Relative air humidity 45 to 75 %
 Before testing the receiver is to be operated on the a.m. conditions for \approx 4 hours
 Voltage variations of power supply \approx \pm 2 %



Receiver setting:

F	10 000.00 kHz
B	1
MOD	4
GC	1

IF $f_{ref} = 200 \text{ kHz} \approx \pm 5 \text{ Hz}$

In case of greater frequency fault:

Correction of the receiver frequency standard (TCXO) with R2410 (reference frequency) on the plug-in rear.

For this, operate the receiver plug-in via a 30-core adapter cable (accessories) outside the casing.

7.1.2. Check and correction on service conditions

- Before testing, the receiver is to be operated at least 2 hours under the a.m. conditions.
- Connect the aerial for receiving a standard frequency transmission 10 MHz or 20 MHz to receiver input socket (29).

unser Eigentum
Verleiher oder
Besitzer wird verifiziert.

101

- Receiver settings:

<input type="checkbox"/> F	according to standard frequency f_N
<input type="checkbox"/> MOD	4
<input type="checkbox"/> B	1
<input type="checkbox"/> GC	5

Control \approx (4) γ

Control \approx (6) γ

- A noise signal changing its volume in the rhythm of the frequency fault is audible in the loudspeaker.

- Admissible frequency fault: $\frac{\Delta f}{f_N} \approx 1 \cdot 10^{-6}/\text{year}$

i.e. with $f_N = 10 \text{ MHz}$ $\Delta f \approx 10 \text{ Hz}$
 $= 20 \text{ MHz}$ $\approx 20 \text{ Hz}$

- Correction of the frequency fault:

Minimize the beat frequency by balancing with R 2419 (reference frequency) on the plug-in rear.

For this, operate the receiver plug-in outside the casing via a 30-core adapter cable (accessories).

102

7.2. Sensitivity

7.2.1. Classes of emission A1A and F1B

- RF generator (P4) to receiver input socket (29)
emf (75 ohm) = 0.5 μ V ($f_G \cong 150$ kHz)
 = 3 μ V ($f_G \cong 150$ kHz)
- AF millivoltmeter (P3) to AF output socket (28)
(measuring range 0.5 V)

- Receiver setting:

F according to test frequency

MOD 1

B 1

GC 5

SEL 0 and 1

\approx \approx

- Tune to maximum with RF generator (P4) at millivoltmeter (P3)
- Adjust level to 250 mV with control \approx (6) at millivoltmeter (P3).
- Measure display decrease (interference voltage spacing in dB) at millivoltmeter after disconnecting the RF generator (P4).

$$\left[\frac{S + R}{R} = 10 \text{ dB} \right]$$

- Repeat measurements for class of emission F1B with MOD 7.

7.2.2. Class of emission A3E

- RF generator (P4) to receiver input socket (29),
emf (75 ohm) = 5 μ V ($m = 0.5$ $f_{MOD} = 1000$ Hz).
- AF millivoltmeter to AF output socket (28), (1.5-V range)

- Receiver setting

A according to test frequency

MOD 2

B 6

GC 5

SEL 0 and 1

~~⚡~~ ≈ ⚡

~~⚡~~ ≈ ⚡

- Tune with RF generator (P4) to 1000 Hz (noise minimum)
- Adjust level to 0,775 V (0 dB) with ~~⚡~~ ≈ at AF millivoltmeter (P 3)
- Disconnect modulation on RF generator (P4) and measure display decrease (noise voltage spacing in dB)

$$\left[\frac{S + R}{R} \approx 10 \text{ dB} \right]$$

7.2.3. Classes of emission J3E, R3E, B8E, B_R3E

- RF generator (P4) to receiver input socket (29),
 emf (75 ohm) = 1.5 μV (EKD 511)
 = 2.2 μV (EKD 512)

- AF millivoltmeter (P3) to AF output (28), 1.5-V range

Observe position A (+ SB) or B (-SB) of the monitoring changeover switch (3).

- Receiver setting:

F according to test frequency

MOD 3,4,5,6

B 7,8

GC 5

SEL 1 and 2

~~⚡~~ ≈ ⚡

~~⚡~~ ≈ ⚡

104

- Tune with RF generator (P4) to 1000-Hz tone
- Adjust level to 0.775 V (0 dB) with $\Delta \approx$ at AF millivoltmeter (P3)
- Disconnect RF generator and measure display decrease (noise voltage spacing in dB) at millivoltmeter

$$\left[\frac{S + R}{R} = 10 \text{ dB} \right]$$

7.2.4. Check of the residual carrier synchronization (R3E and E_R8E)


- RF generator (P4) to receiver input socket (29)
emf (75 ohm) = 1 μ V
- Receiver setting:

F according to test frequency

MOD 5, 6

GC 5

$\Delta \approx \gamma$
 $\Delta \approx \gamma$

- Tune to zero beat with RF generator (P4)
- Check display  (11) for residual carrier synchronization shall light in the detuning range $\Delta f = \pm 50 \text{ Hz}$.

Dieser Empfänger
 ist ein Eigentum
 der Bundeswehr
 und darf nicht
 weitergegeben
 werden.

Dieser Empfänger
 ist ein Eigentum
 der Bundeswehr
 und darf nicht
 weitergegeben
 werden.

7.3. Amplification control (17A) ~~EMF generator~~ (29) (25) (26)

7.3.1. Manual control 'basic amplification'

- RF generator (P4) to receiver input socket (29),
emf (75 ohm) = 1 μ V
- AF millivoltmeter (P3) to line outputs A (25) or B (26) terminated with 500 ohm, 1,5-V range.
- Receiver setting:

F	4 500.00 kHz
MOD	6
B	6
GC	5
SEL	0

~~X~~ \approx γ

- Tune with RF generator (P4) to 1000-Hz tone in AF channel B or A and read test values on AF millivoltmeter.

Setpoint values: 0.775 V \pm 1 dB

- Correction of the AF output level

Channel A : with R 3847	}	cassette 'signal path 2'
Channel B : with R 3617		

- Check of the display 'U \approx ' on LED row (12).
Monitoring changeover switch (3) \rightarrow 'U \approx '

7.3.2. Manual control 'synchronism, control volume'

(Test arrangement as with Section 7.3.1.)

- Increase emf of the RF generator from 1 μ V to 1V in 20-dB steps, level at AF line output B (26) to 0 dBm each by means of and compare level with AF line output A (25) \rightarrow 2-kHz step.

196

3 wird verlegt.

Setpoint values: synchronism $\frac{U_{AF} 'A'}{U_{AF} 'B'} = \pm 2 \text{ dB}$

control volume = 120 dB (setting to 0 dBm)

- Correction of synchronism ($U_{AF} 'A'$) with R. 3734 (signal path 2).

7.3.3. Automatic control 'synchronism, control volume'

(Test arrangement as with Section 7.3.1. GC 1)

- Increase emf of the RF generator from 2 μV to 200 mV in 20-dB steps and measure AF level at every time at line output A (25) and B (26).

Setpoint values: synchronism $\frac{U_{AF} 'A'}{U_{AF} 'B'} = \pm 2 \text{ dB}$

control volume = 0.775 V $\pm 3 \text{ dB}$

- Correction: $U_{AF} 'A'$ with R 3801 }
 $U_{AF} 'B'$ with R 3616 } signal path 2

7.3.4. Automatic control 'digital display of the receiving signal'

- Receiver setting:

F 4 500.00 kHz

MOD 1

B 2

GC 1

SEL 0

Changeover switch 'LED row' \rightarrow E \rightarrow

A-D converter test A 3

(EXT EXT \leftarrow 1.5 s \rightarrow

ohne Egektor
 fällung nach
 wird befolgt

11/1987

- Turn LED row to maximum with RF generator (emf = 100 μ V)
- Increase emf values from 1 μ V (\approx 0 dB μ V) to 1 V (\approx 120 dB μ V) in 10-dB steps.
- Doubly indicated digit value \approx dB μ V (tolerance: \pm 2)
(e.g.: 30 \approx 60 dB μ V \approx 1 mV)
- Simultaneously with that: Check display value on LED row
(tolerance: \pm 1 LED)

8. Components selected by the manufacturer

Repair work on some circuits of the receiver requires particularly pretested or prepared (programmed) components which can be ordered from the manufacturer of the equipment.

V3304 Si-Schottky diode quartette 4 KAS 34
($\Delta U_F \cong 20$ mV at $I_F = 1 \dots 7$ mA, $\Delta C_o \cong 0,2$ pF)

V3305, V3306 } Transistor pairs SF235
V3309, V3310 } acc. to 1340.041-01353 Pv 2
V3311, V3312 } ($\Delta I_C \cong 10$ % at $I_B =$ constant,
V3402, V3403 } $U_{CE} = 4.5$ V, $I_C =$ approx. 5 mA)

V3405, V3406 FET KP307 A
acc. to 1340.041-01354 Pv 3
($U_{\text{pinch-off}} = -0.8 \dots -1.3$ V at $I_D = 100$ μ A,
 $U_{DS} = 10$ V)

N3602, N3704 Circuit pair A281 D
acc. to 1340.037-01356 Pv 2
01357
($\Delta V \cong 2$ dB within the control range)

V3601, V3701, V3704 FET KP307 A
acc. to 1340.041-01345 Pv 3
($I_D > 100$ μ A at $U_{DS} = 10$ V,
 $U_{\text{pinch-off}} = -1.3$ V)

V2209...V2212 Si diode quartette SAY17
acc. to 1340.037-01253 Pv 2
($C_o \cong 1.5$ pF at 10 MHz)

V2104, V2106, } FET KP307 A
V2108, V2113, } acc. to 1340.037-01251 Pv 2
V2115, V2301, }
V2312, V2504 } Group 3...7, ($I_D = 3$ mA, $U_{GS} = 0.33 \dots 1.1$ V
V2506, V2508, } $/Y_{21S}/ = 3.5$ mS at 20 kHz)
V2513 }

V2105, V2505 FET KP307 A
acc. to 1340.037-01251 Pv 2
Group 9...11 ($I_D = 3$ mA, $U_{GS} = 2 \dots 4$ V
 $/Y_{21S}/ = 3.5$ mS at 20 kHz)

D4408...D4411 Circuit U2716C 65 (EPROM)
programmed acc. to 1340.041-01454 Bv
Indicate program-No., e.g. progr. 2/1...4.